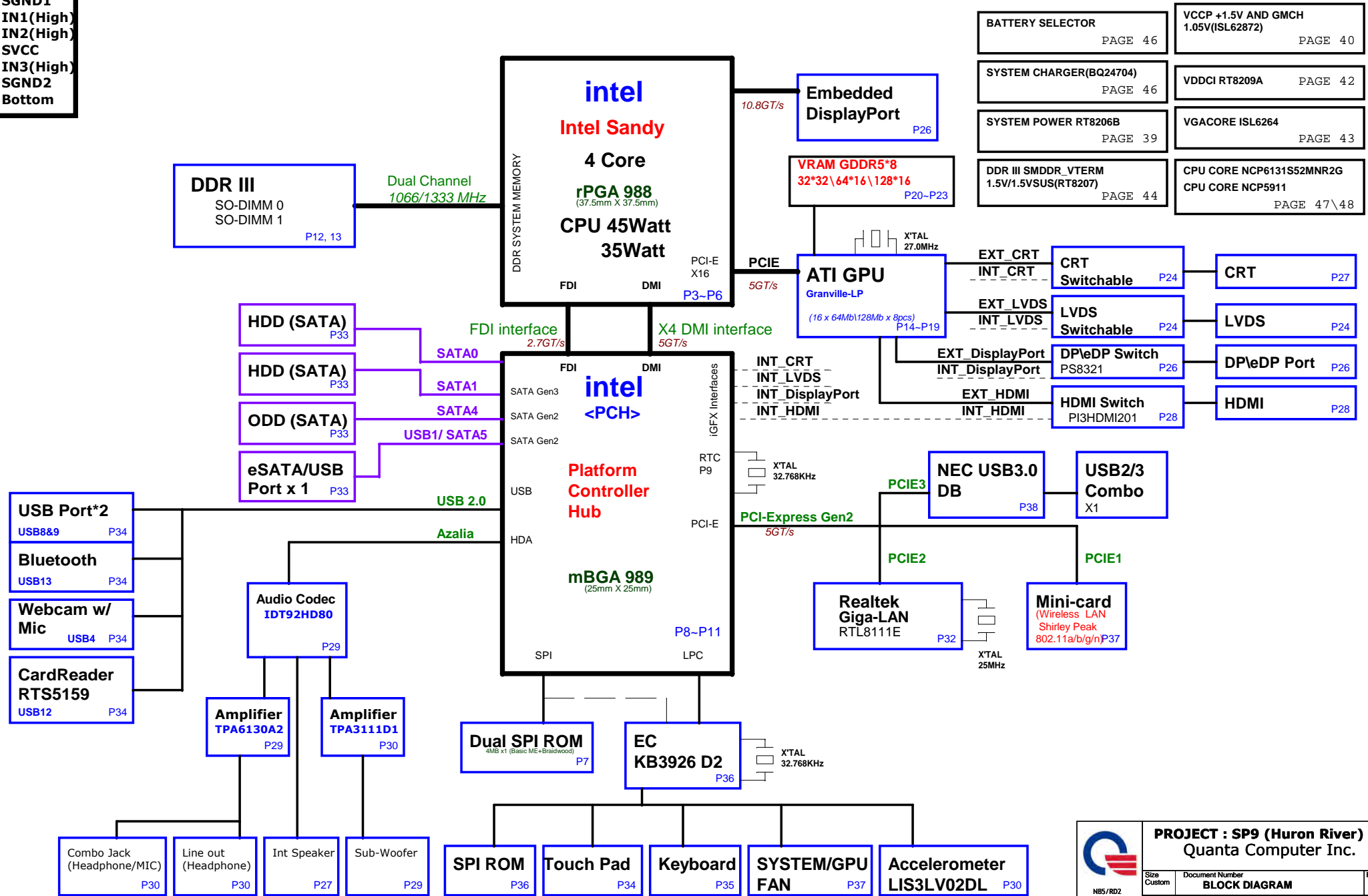
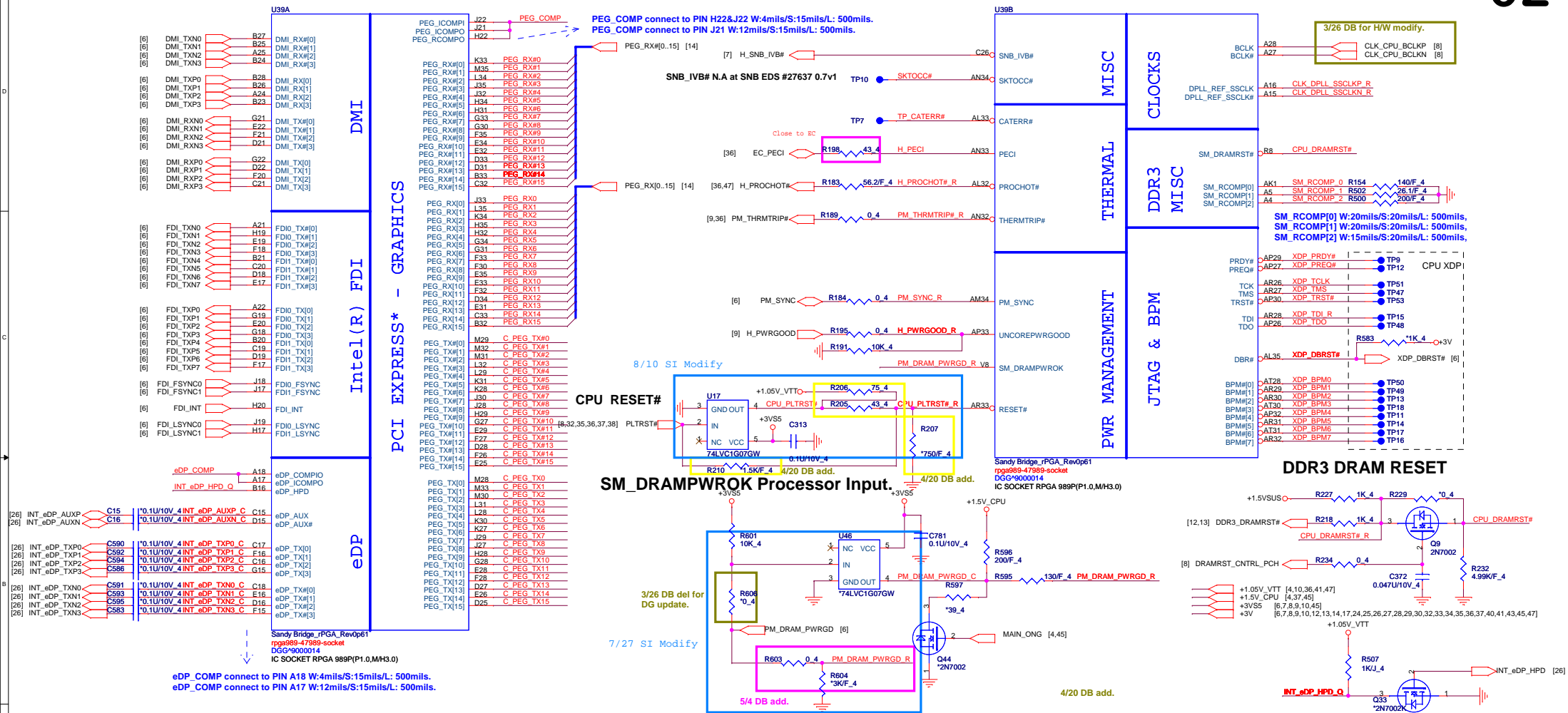


LAYER 1 : TOP
 LAYER 2 : SGND1
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(High)
 LAYER 5 : SVCC
 LAYER 6 : IN3(High)
 LAYER 7 : SGND2
 LAYER 8 : Bottom

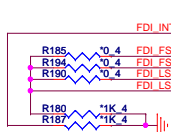
SP9 BLOCK DIAGRAM

01



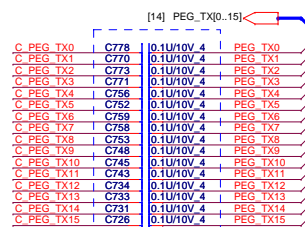


FDI disable (DIS only stuff)

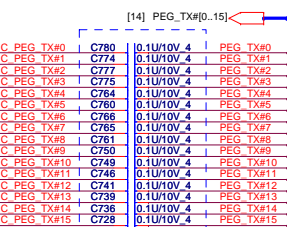


FDI_DISABLE can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

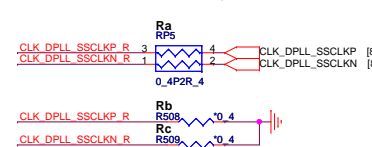


0.22uF AC coupling Caps for PCIe GEN1/2/3



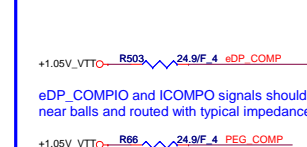
0.22uF AC coupling Caps for PCIe GEN1/2/3

Embedded Display PLL Clock



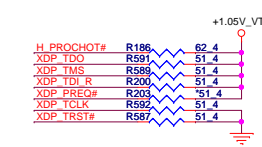
	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation\ Hot-plug



PEG_DISABLE and PEG_DISABLE# signals should be shorted near balls and routed with typical impedance <25 mohms

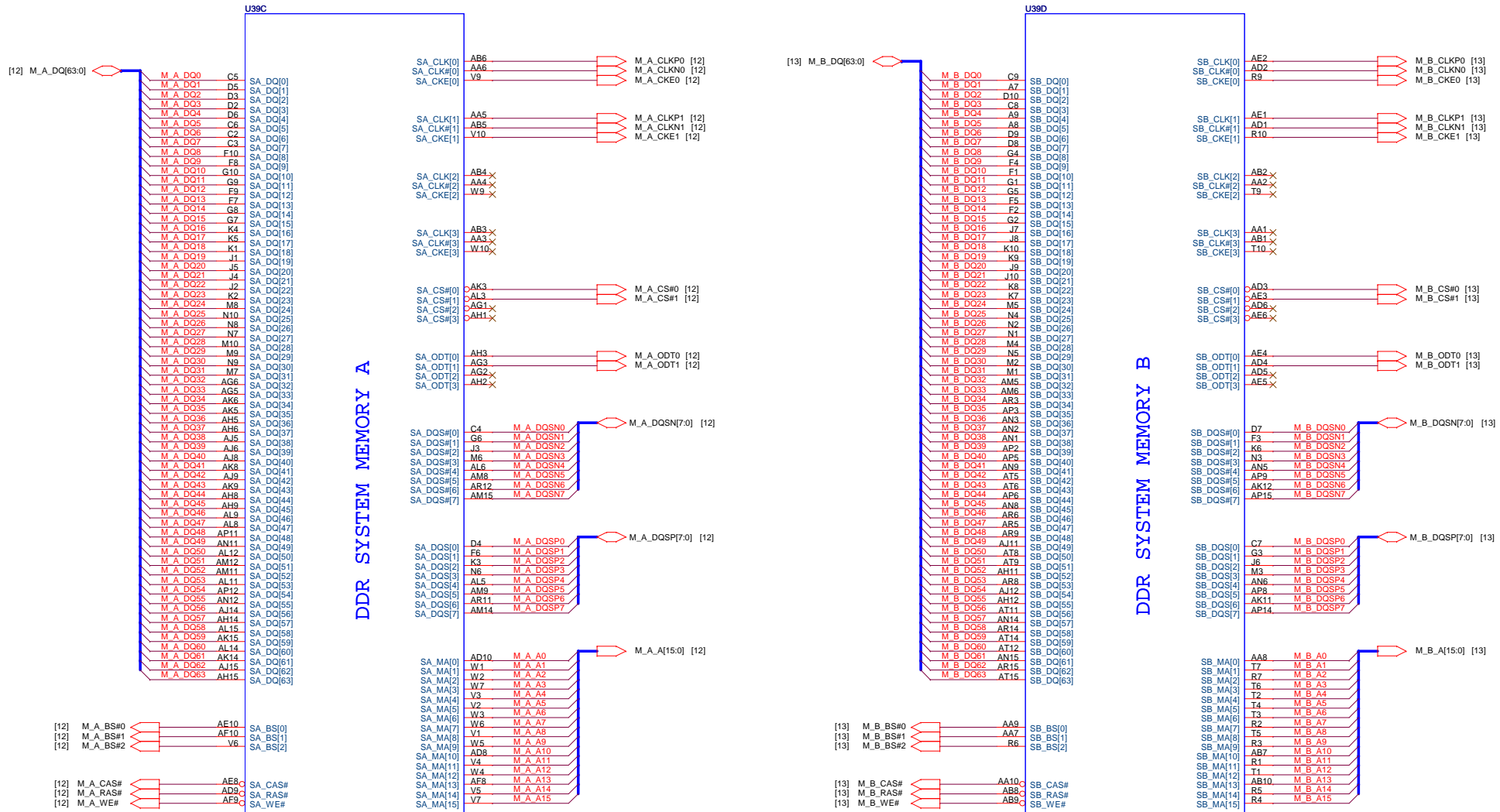
Processor pull-up (CPU)



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A
Date: Tuesday, August 10, 2010	Sheet 2 of 49	

Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

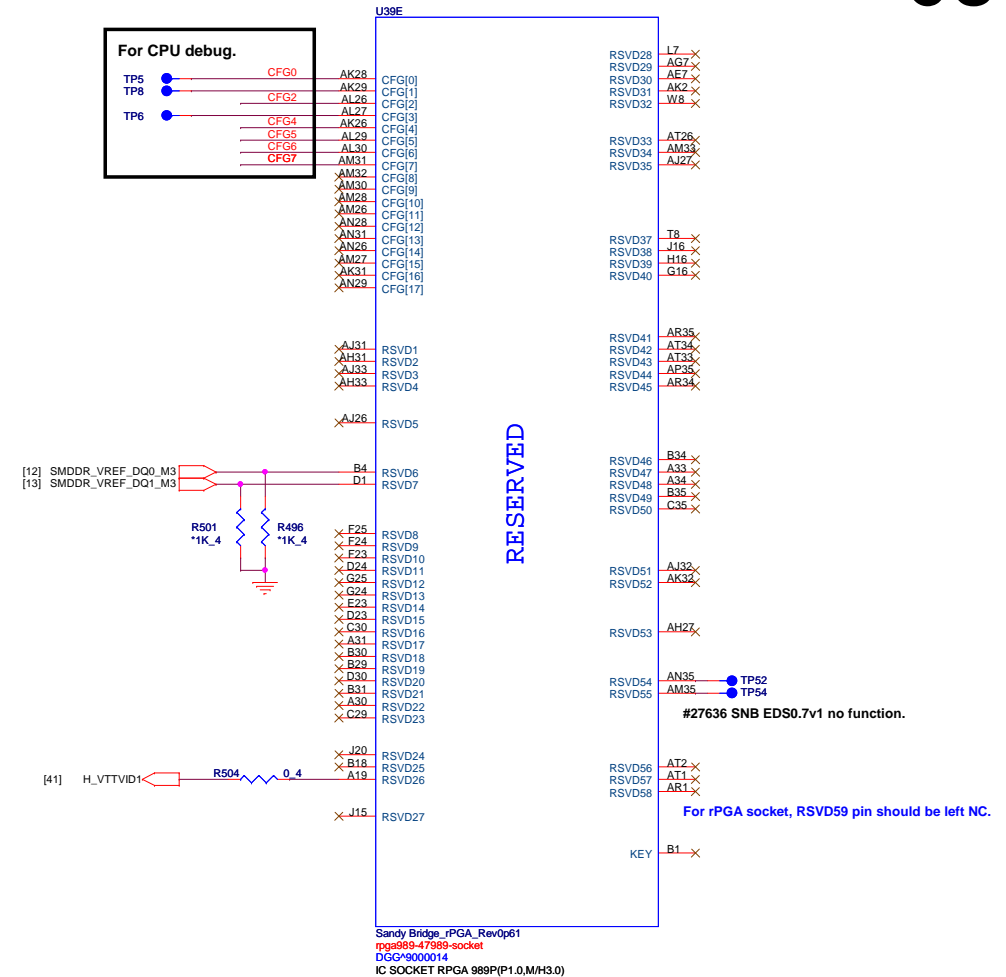
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)



Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



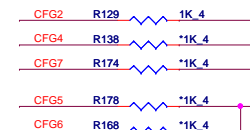
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIe Port Bifurcation Straps)

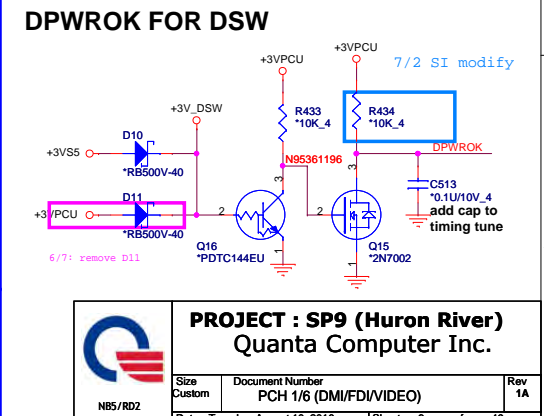
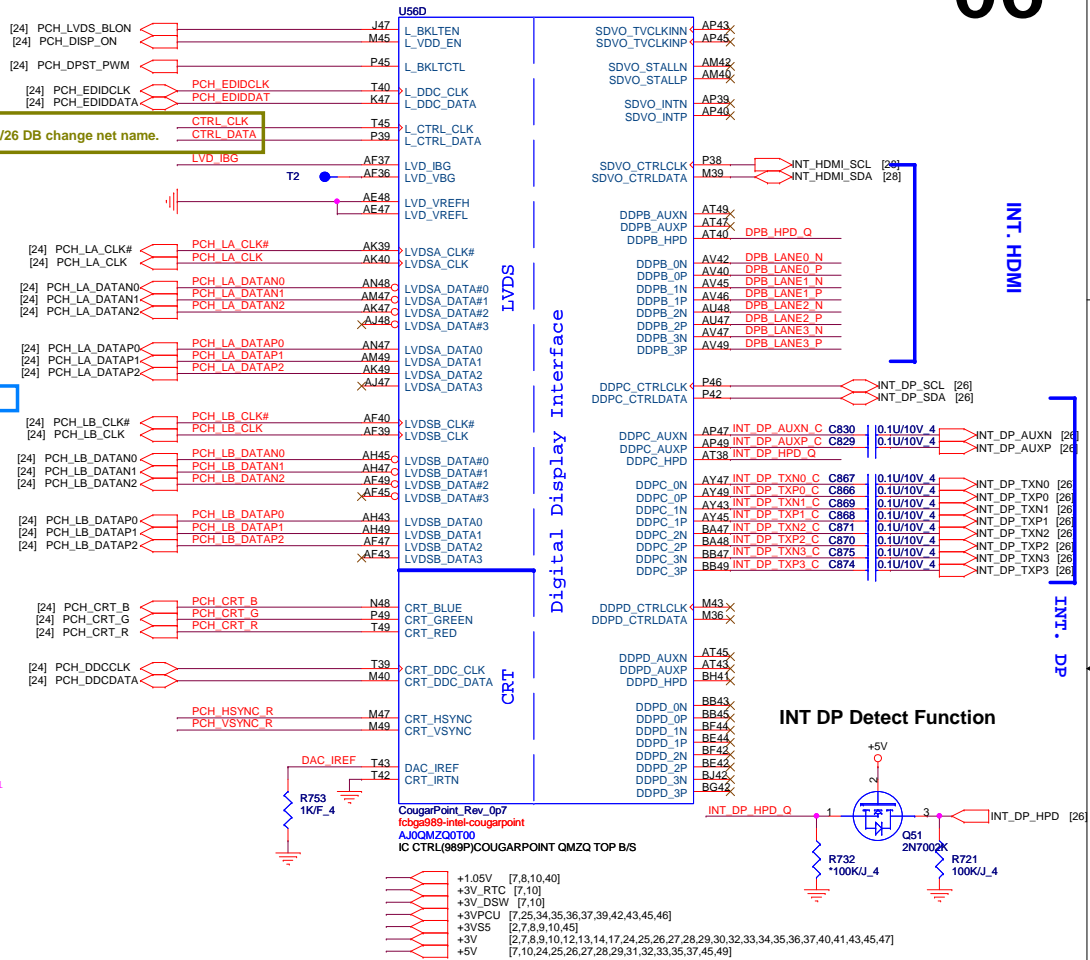
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



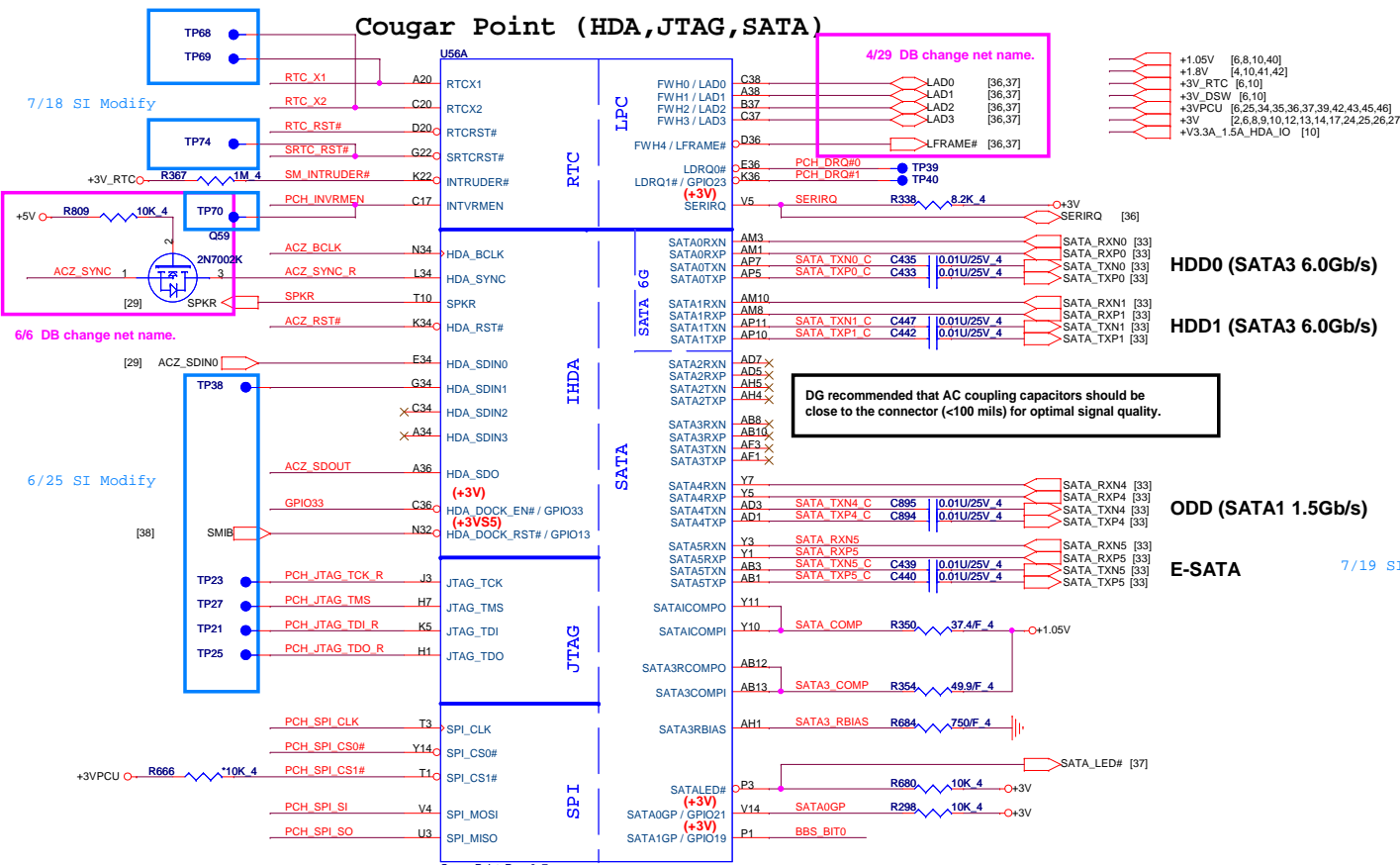
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom Document Number SNB 4/4 (GND) Rev 1A

Date: Tuesday, August 10, 2010 Sheet 5 of 49

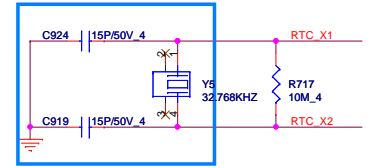


Cougar Point (HDA,JTAG,SATA)



8/1 SI modify

RTC Clock 32.768KHz



HDD0 (SATA3 6.0Gb/s)

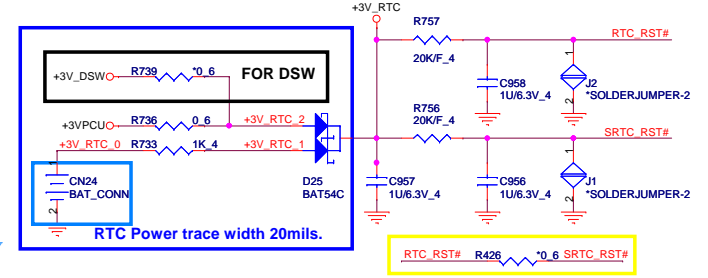
HDD1 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

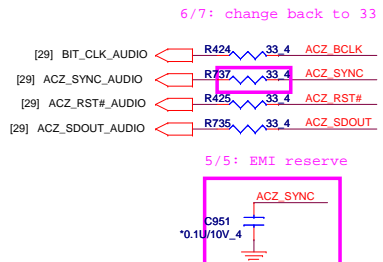
E-SATA

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

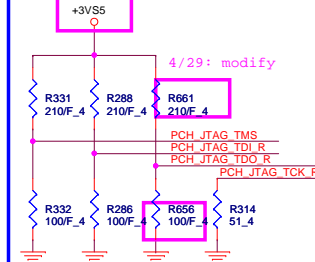
RTC Circuitry(RTC)



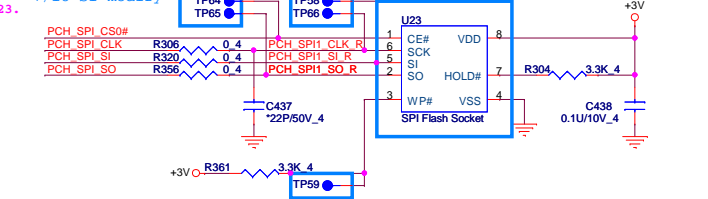
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

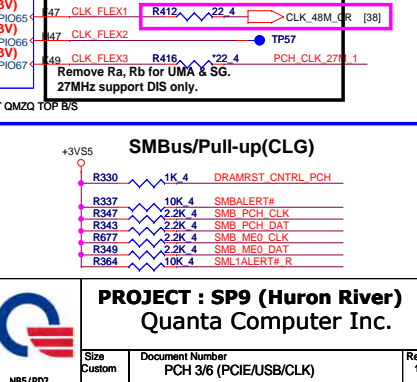
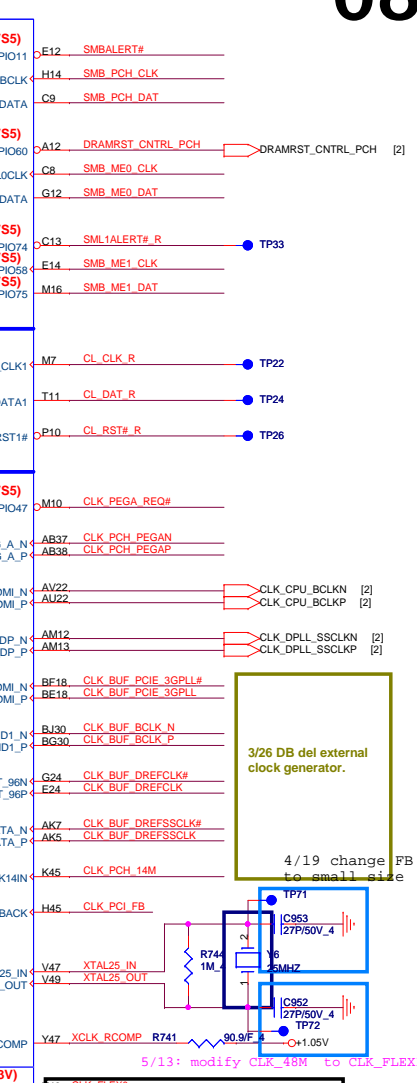
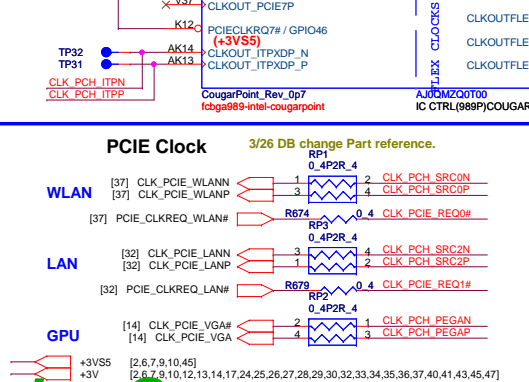
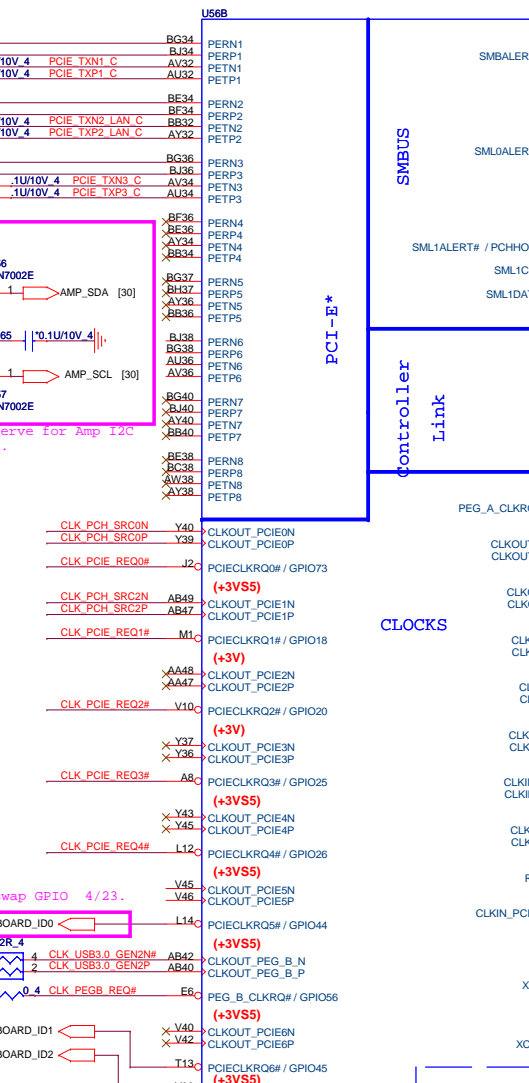
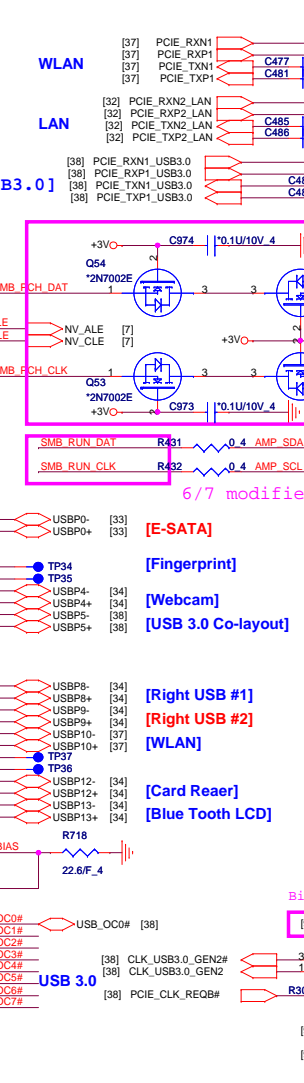
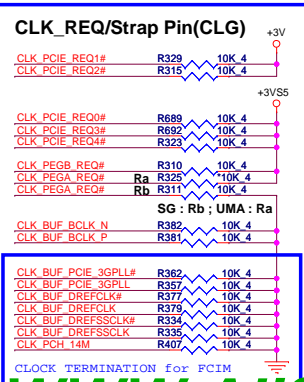
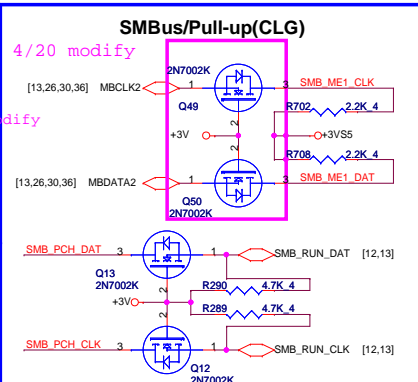
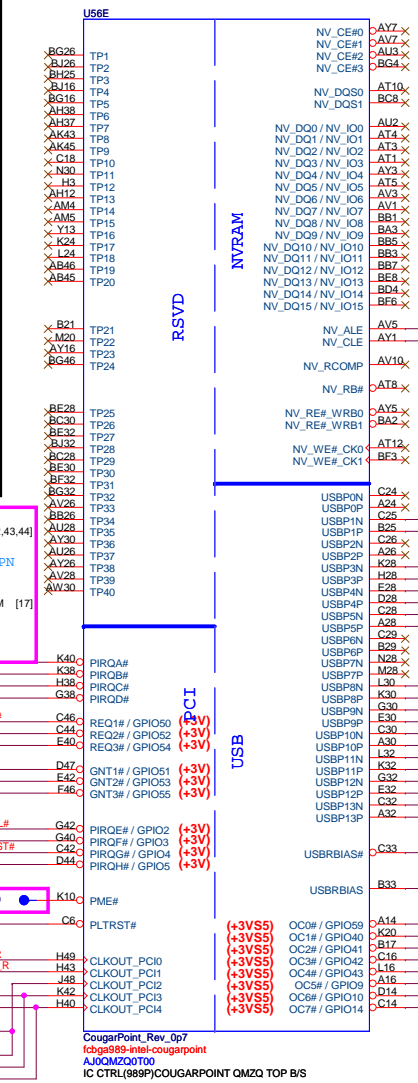
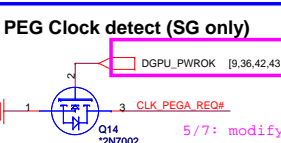
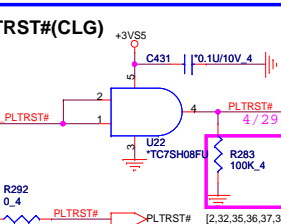
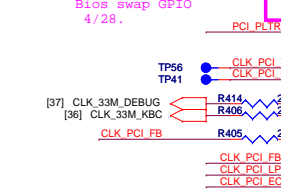
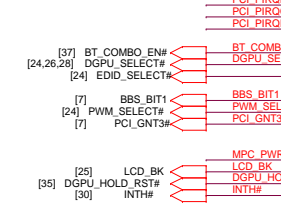
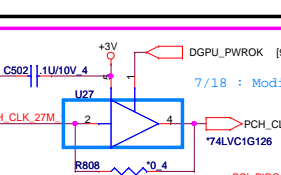
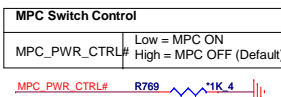
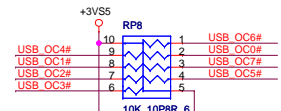
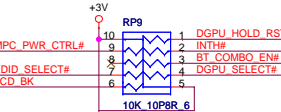
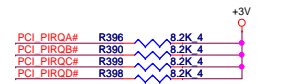
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R660 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R749 R746 *1K 4 +3V PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R716 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R727 1K 4 GPIO33_E [36]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R667 R752 *1K 4 BBS_BIT0 [8]
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	USE GPIO PIN +1.8V R691 *1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R678 2.2K 4 R694 4.7K 4 NV_CLE [8]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R734 *1K 4 ACZ_SYNC_R 5/4 add
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R738 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R703 *1K 4 4/29 reserve. ICC_EN# [9]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R693 *1K 4 PLL_ODVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R308 1K 4 +3V

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

PCI/USBOC# Pull-up(CLG)



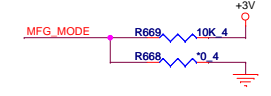
Cougar Point (GPIO,VSS_NCTF,RSVD)



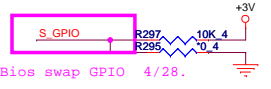
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

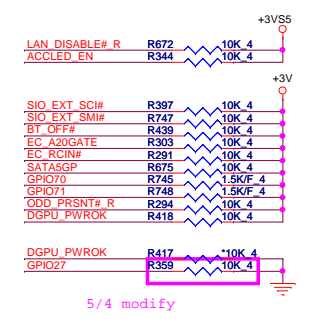
MFG-TEST



SGPIO



GPIO Pull-up/Pull-down(CLG)



RF_OFF#

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

BIOS RECOVERY

High = Disable (Default)

Low = Enable

TEST_SET_UP

SV_SET_UP

High = Strong (Default)

TEST DETECT

Low = Default

DGPU_PWR_EN_R

DMI TERMINATION VOLTAGE OVERRIDE

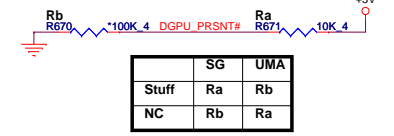
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI_OVRVLTS

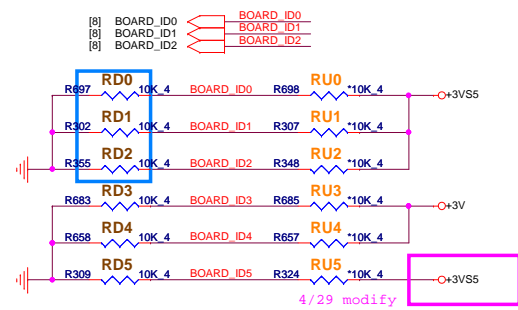
FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

GFX Present



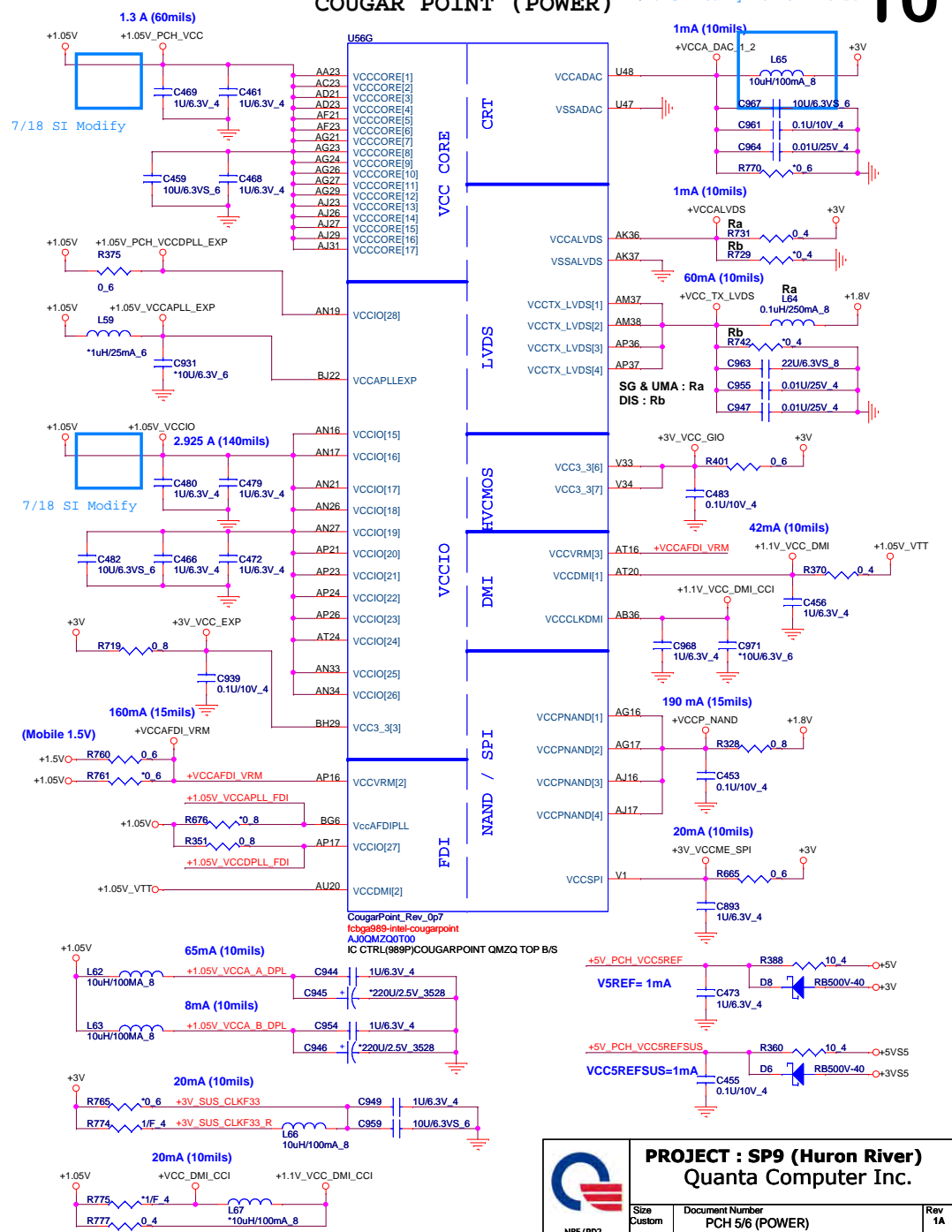
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
SP9 2D	0	0	0	0	0	0
SP9 3D	0	0	0	0	0	1



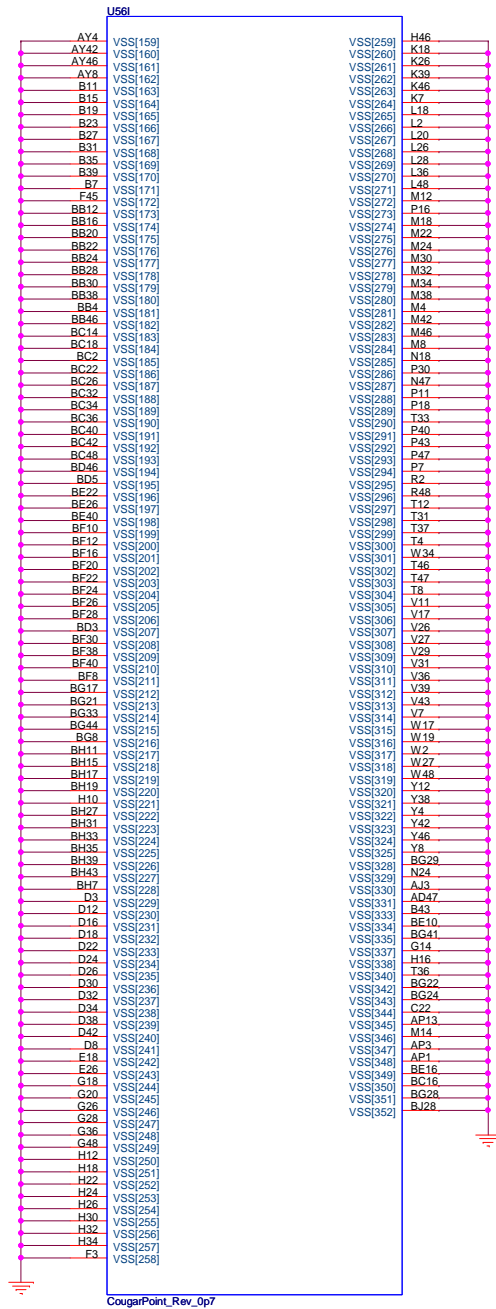
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Tuesday, August 10, 2010		Sheet 9 of 49

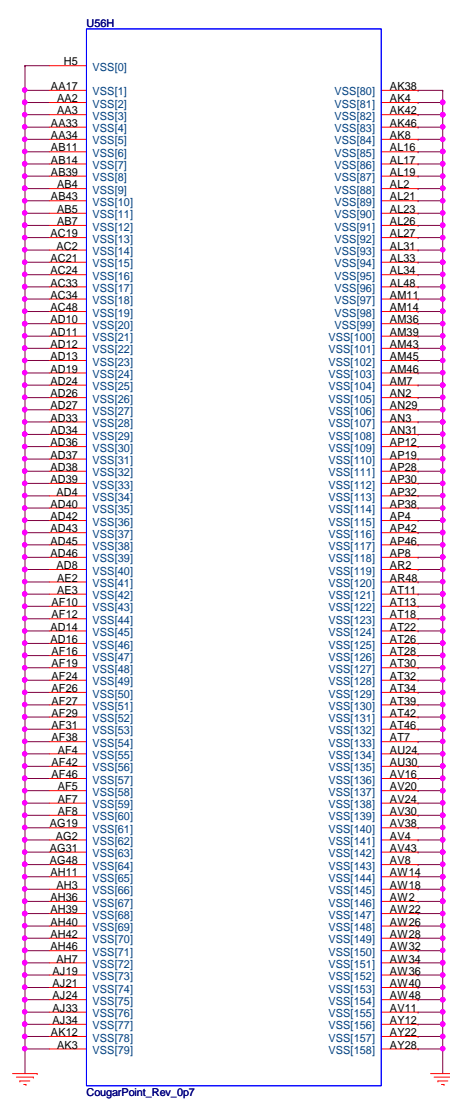
COUGAR POINT (POWER)

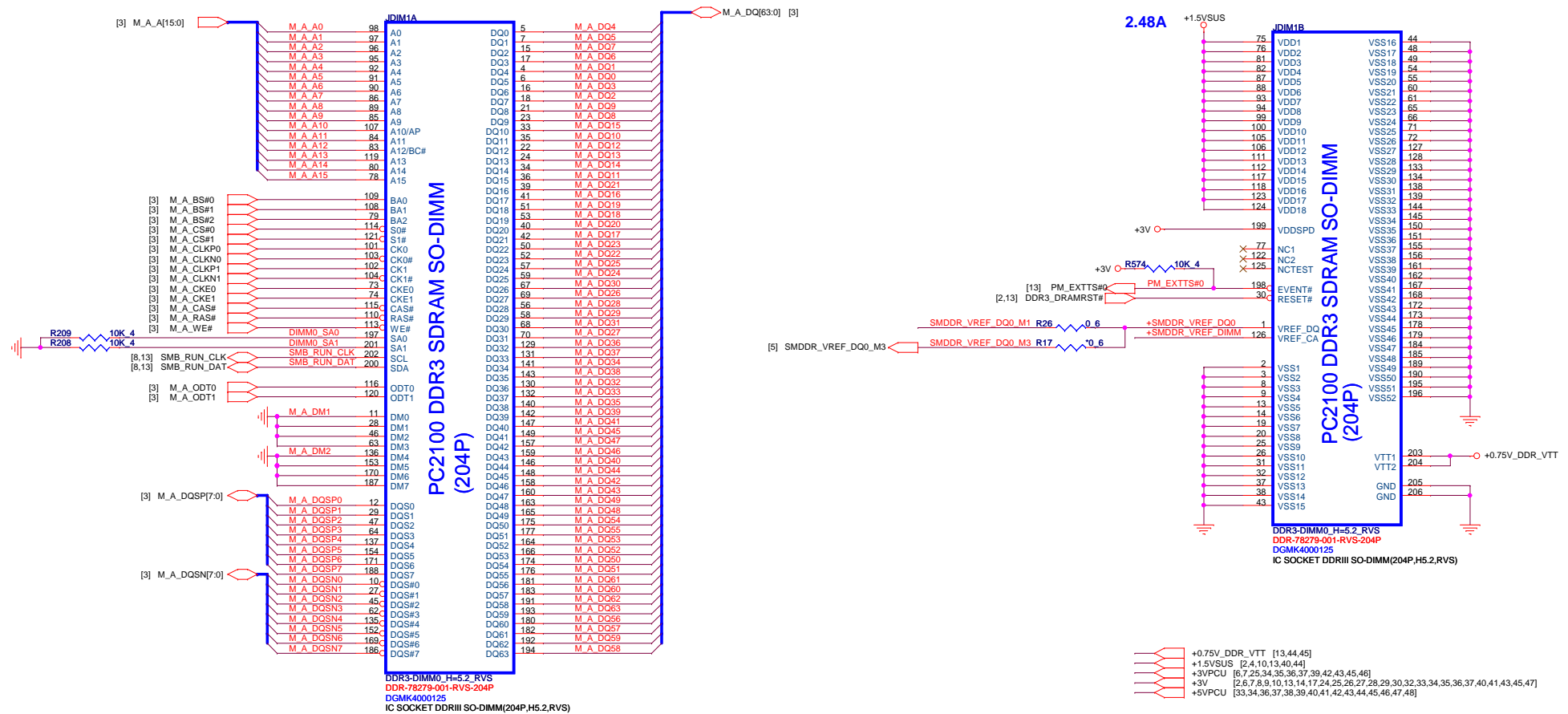


IBEX PEAK-M (GND)



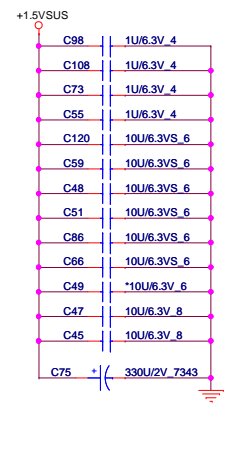
IBEX PEAK-M (GND)



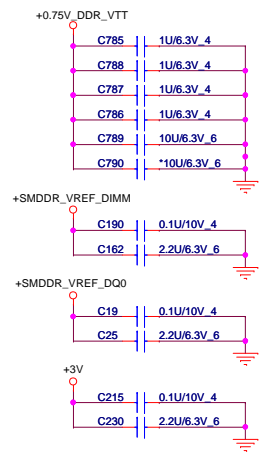


7/18 : Del M2 solution

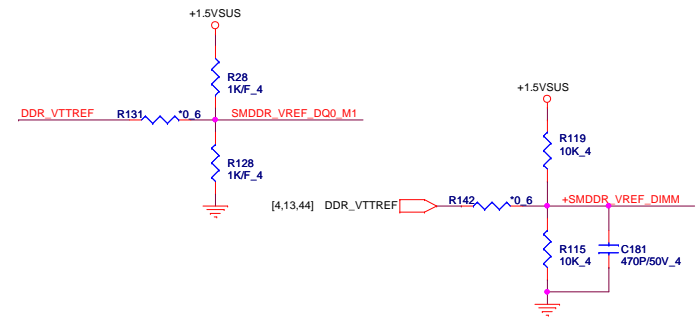
VREF DQ0 M2 Solution




Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution

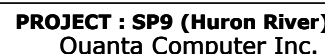
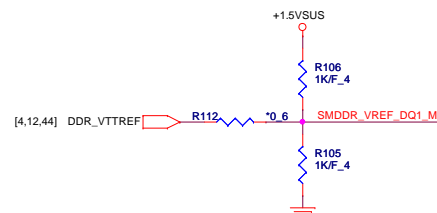
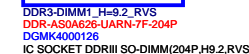
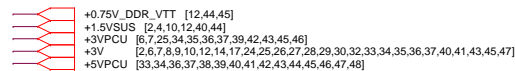


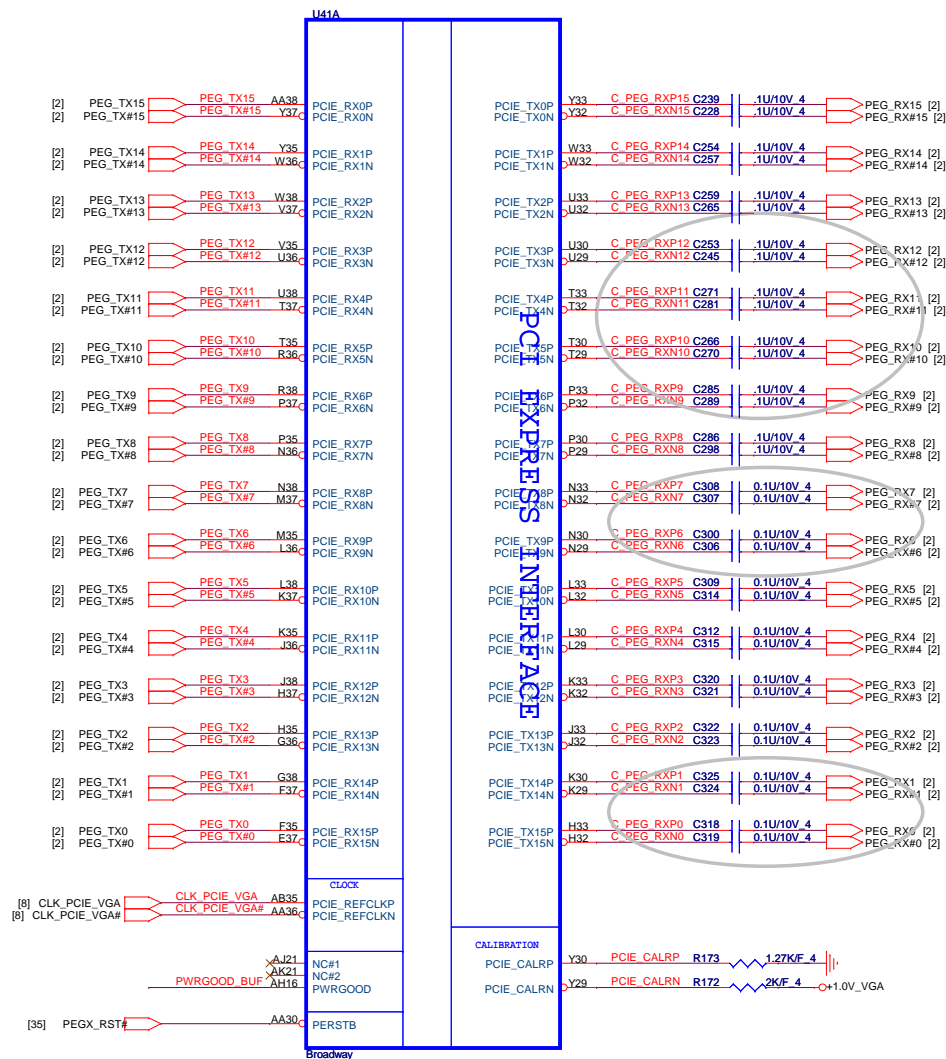


NBS/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A
Date: Tuesday, August 10, 2010		Sheet 12 of 49

NB5/RD2

for DB2

U41H

DP C/D POWER
+1.8V_DPC_VDD18 AP20 DPC_VDD18#1 AP21 DPC_VDD18#2
+1.0V_DPC_VDD10 AP13 DPC_VDD10#1 AT13 DPC_VDD10#2
DPC_VSSR#1 AN17
DPC_VSSR#2 AP16
DPC_VSSR#3 AP17
DPC_VSSR#4 AW14
DPC_VSSR#5 AW16

DP A/B POWER
+1.8V_DPA_VDD18 AN24 DPA_VDD18#1 AP24 DPA_VDD18#2
+1.0V_DPA_VDD10 AP31 DPA_VDD10#1 AP32 DPA_VDD10#2
DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26

DPB_VDD18#1 AP25
DPB_VDD18#2 AP26
DPB_VDD10#1 AN33
DPB_VDD10#2 AP33

DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32

DPD_VDD18#1 AP22
DPD_VDD18#2 AP23
DPD_VDD10#1 AP14
DPD_VDD10#2 AP15

DPD_VSSR#1 AN19
DPD_VSSR#2 AP18
DPD_VSSR#3 AP19
DPD_VSSR#4 AW20
DPD_VSSR#5 AW22

DPD_CALR R45 150/F 4 DPCD_CALR AW18
DPAB_CALR AW28 DPAB_CALR R539 150/F 4

DP PLL POWER
+1.8V_VGA AU28 DPA_PVDD AU27 DPA_PVSS
+1.8V_DPB_PVDD AV29 DPB_PVDD AV28 DPB_PVSS
DPC_PVDD AU18 DPC_PVSS AV17
DPD_PVDD AV19 DPD_PVSS AR18
DPE_PVDD AM37 DPE_PVSS AN38
DPF_PVDD AL38 DPF_PVSS AM35

(DPA/B_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
C119 10U/6.3V_8 C135 1U/6.3V_4 .1U/10V_4
HCB1608KF-181T15.6 L13

(DPB_PVDD : 1.8V@20mA) +1.8V_VGA
C653 10U/6.3V_8 C658 1U/6.3V_4 C659 .1U/10V_4
HCB1608KF-181T15.6 L50

(DPC_PVDD : 1.8V@20mA) +1.8V_VGA
C625 10U/6.3V_8 C637 1U/10V_4 C632 1U/6.3V_4
HCB1608KF-181T15.6 L44

(DPD_PVDD : 1.8V@20mA) +1.8V_VGA
C648 10U/6.3V_8 C660 1U/10V_4 C655 1U/6.3V_4
HCB1608KF-181T15.6 L47

(DPE/P_VDD1.8V@20mA+20mA) +1.8V_VGA
C670 10U/6.3V_8 C671 1U/10V_4 C672 1U/10V_4
HCB1608KF-181T15.6 L51

(DPE/F_VDD18 : 1.8V@200mA+200mA) +1.8V_VGA
C165 10U/6.3V_8 C166 1U/6.3V_4 C167 .1U/10V_4
HCB1608KF-181T15.6 L12

(DPA/B_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
C636 10U/6.3V_8 C644 1U/6.3V_4 C647 .1U/10V_4
HCB1608KF-181T15.6 L46

(DPC/D_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
C107 10U/6.3V_8 C661 1U/6.3V_4 C656 .1U/10V_4
HCB1608KF-181T15.6 L9

(DPC/D_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
C643 10U/6.3V_8 C635 1U/6.3V_4 C634 .1U/10V_4
HCB1608KF-181T15.6 L11

DPEF_CALR R545 150/F 4 DPEF_CALR AM39

Broadway

for AMD comment add for SI

For future ASIC, if PWRGOOD_BUF is not required it should be pulled to ground.

U4 MC74VHC1G08DFT2G
R52 10K_4
R53 10K_4
PWRGOOD_BUF

[36,39,40,41,44,49] HWPG

(DPE/F_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
C123 10U/6.3V_8 C126 1U/6.3V_4 C127 .1U/10V_4
HCB1608KF-181T15.6 L12

(DPA/B_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
C636 10U/6.3V_8 C644 1U/6.3V_4 C647 .1U/10V_4
HCB1608KF-181T15.6 L46

(DPC/D_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
C107 10U/6.3V_8 C661 1U/6.3V_4 C656 .1U/10V_4
HCB1608KF-181T15.6 L9

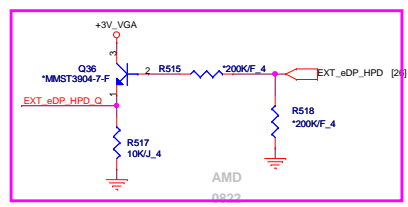
(DPC/D_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
C643 10U/6.3V_8 C635 1U/6.3V_4 C634 .1U/10V_4
HCB1608KF-181T15.6 L11

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number ATI M97-M2 (PCIE I/F) 1/5	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 14 of 49	

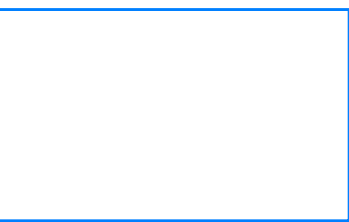
WWW.AliSaler.Com





5/6 DB add.

7/19 SI Modify remove R541/R51/C664/C50



5/6 add for AMD

For LVDS

reserver for internal thermal

PV change for EC request

5/20 add for AMD

PV Add CTF function.

3D support

3D support

Place VREFG Divider and CAP close to ASIC

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

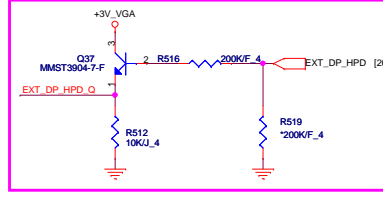
3D support

3D support

3D support

3D support

3D support



5/6 DB add.

HDMI

3D support

eDisplay port

Mini-display port

Mini-display port

Mini-display port

Mini-display port

Mini-display port

Mini-display port

Mini-display port

Mini-display port

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Mini-display port

Mini-display port

Mini-display port

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Mini-display port

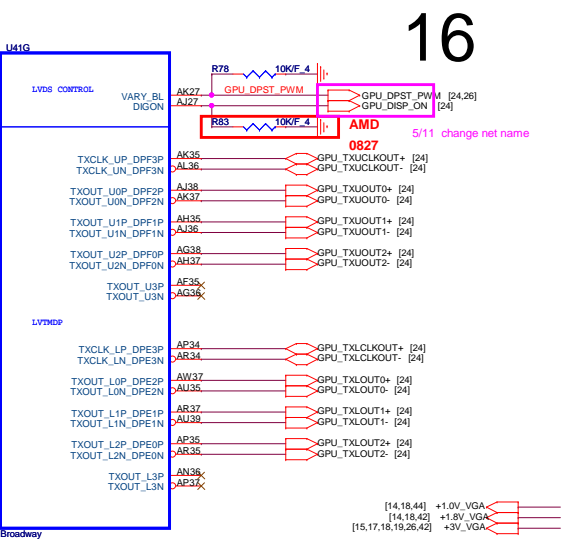
Mini-display port

Mini-display port

Mini-display port

Mini-display port

Mini-display port



7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

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7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

7/19 SI Modify to fix CRT noise

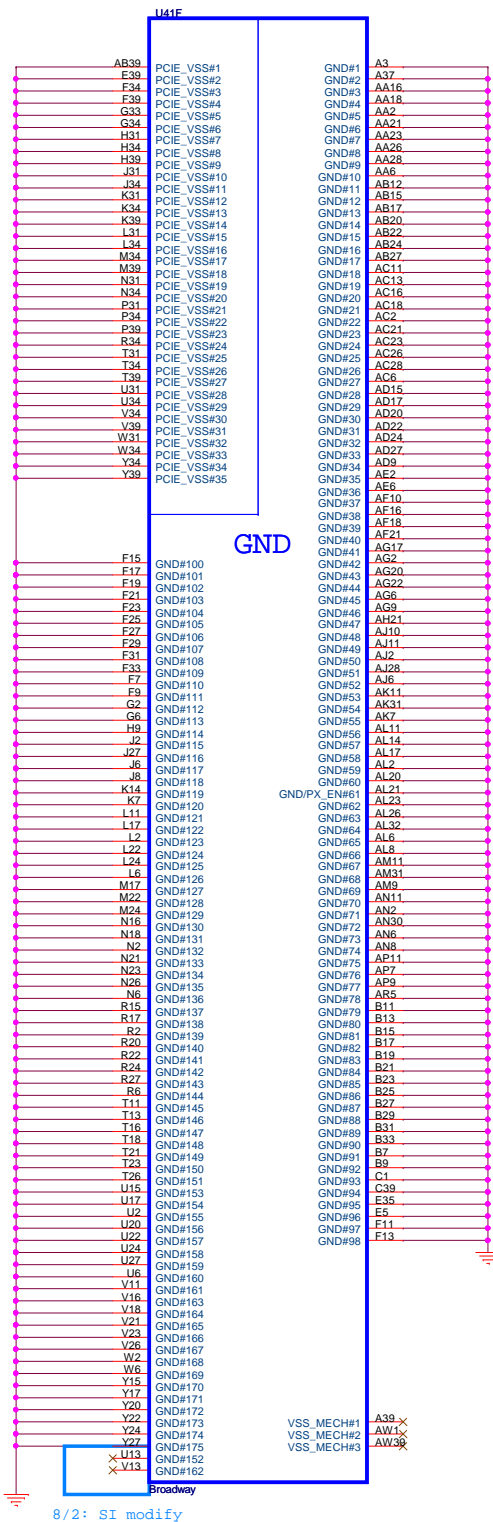
7/19 SI Modify to fix CRT noise

MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	DDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-TOC BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-TOC BGA (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC05 (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G

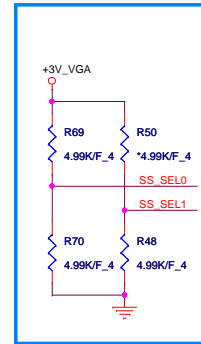
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom Document Number ATI M97-M2 (DISPLAY) 3/5 Rev 1A

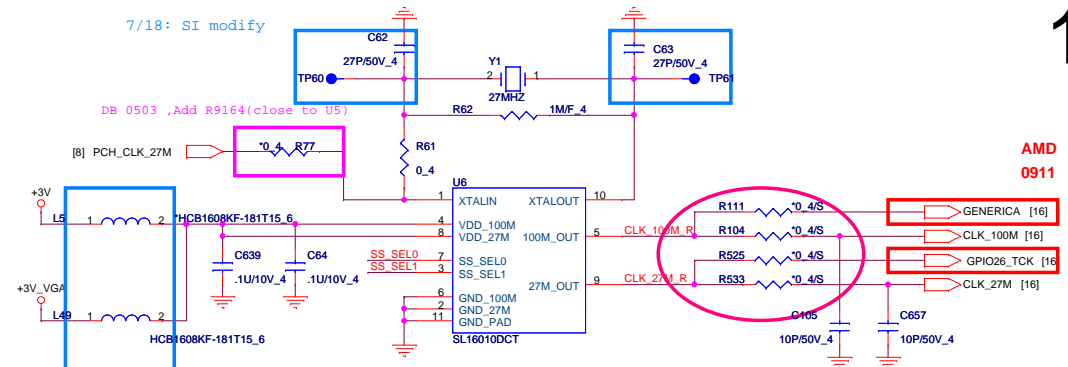
Date: Tuesday, August 10, 2010 Sheet 16 of 49



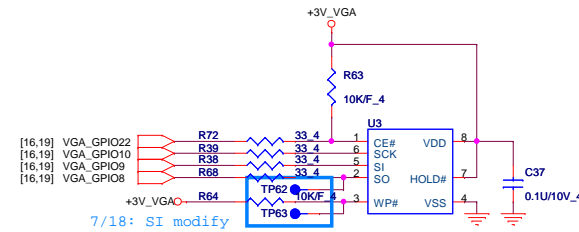
27MHz + 100Mhz OSC Option



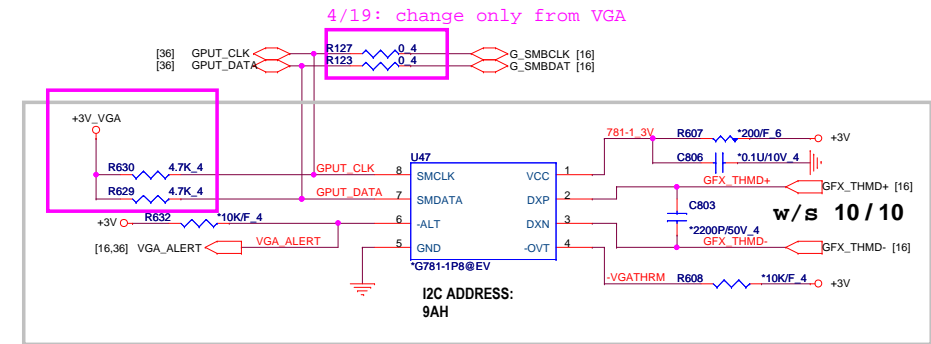
7/18: SI modify



Ext EEPROM



Thermal Sensor



[2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

[15,16,18,19,26,42]



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	1A
Date: Tuesday, August 10, 2010	Sheet 17 of 49	



Straps

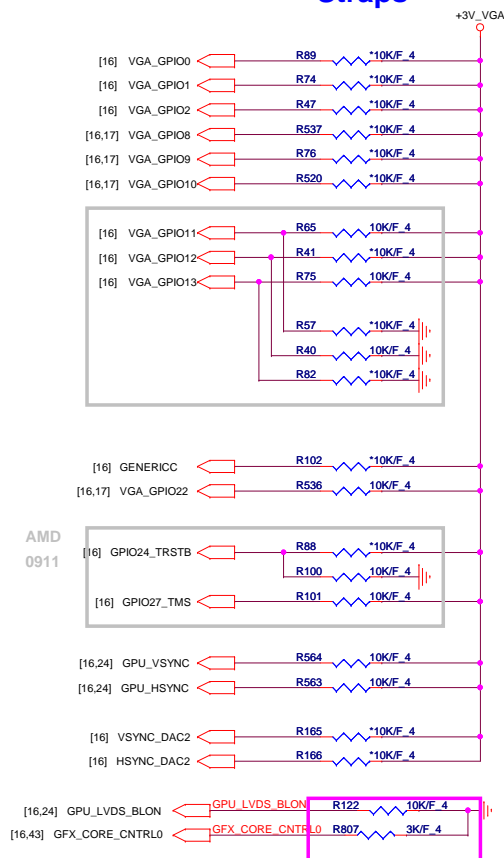


Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

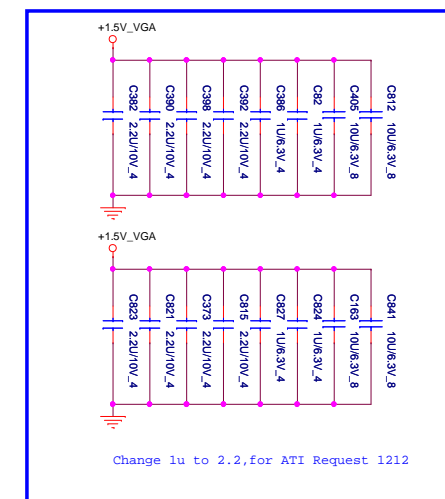
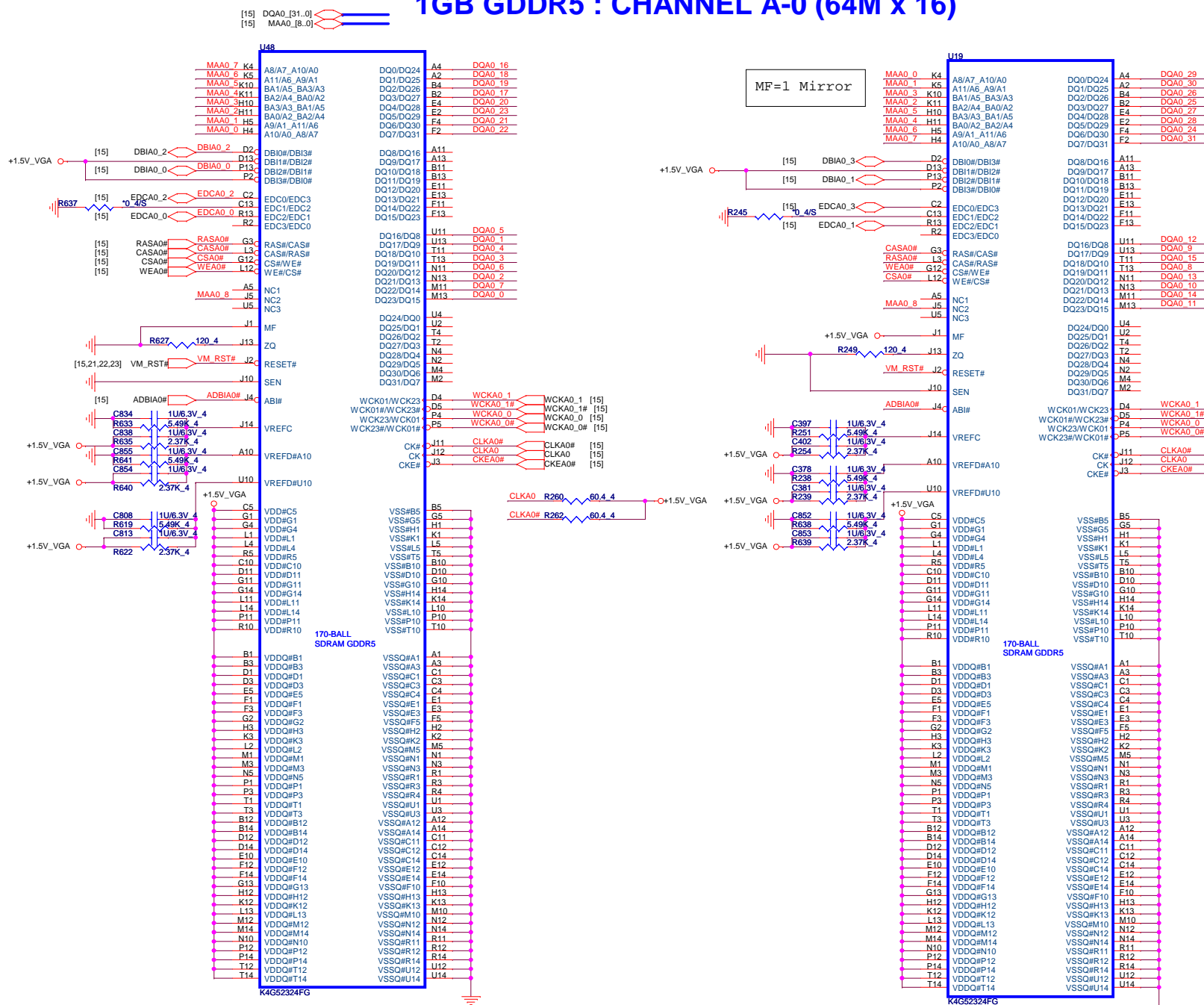
Strap Name	Pin	Straps Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYN		
AUD(1)	HSYN		
VSYN_DAC2	V2SYN		
HSYN_DAC2	H2SYN		
	GENERICC		



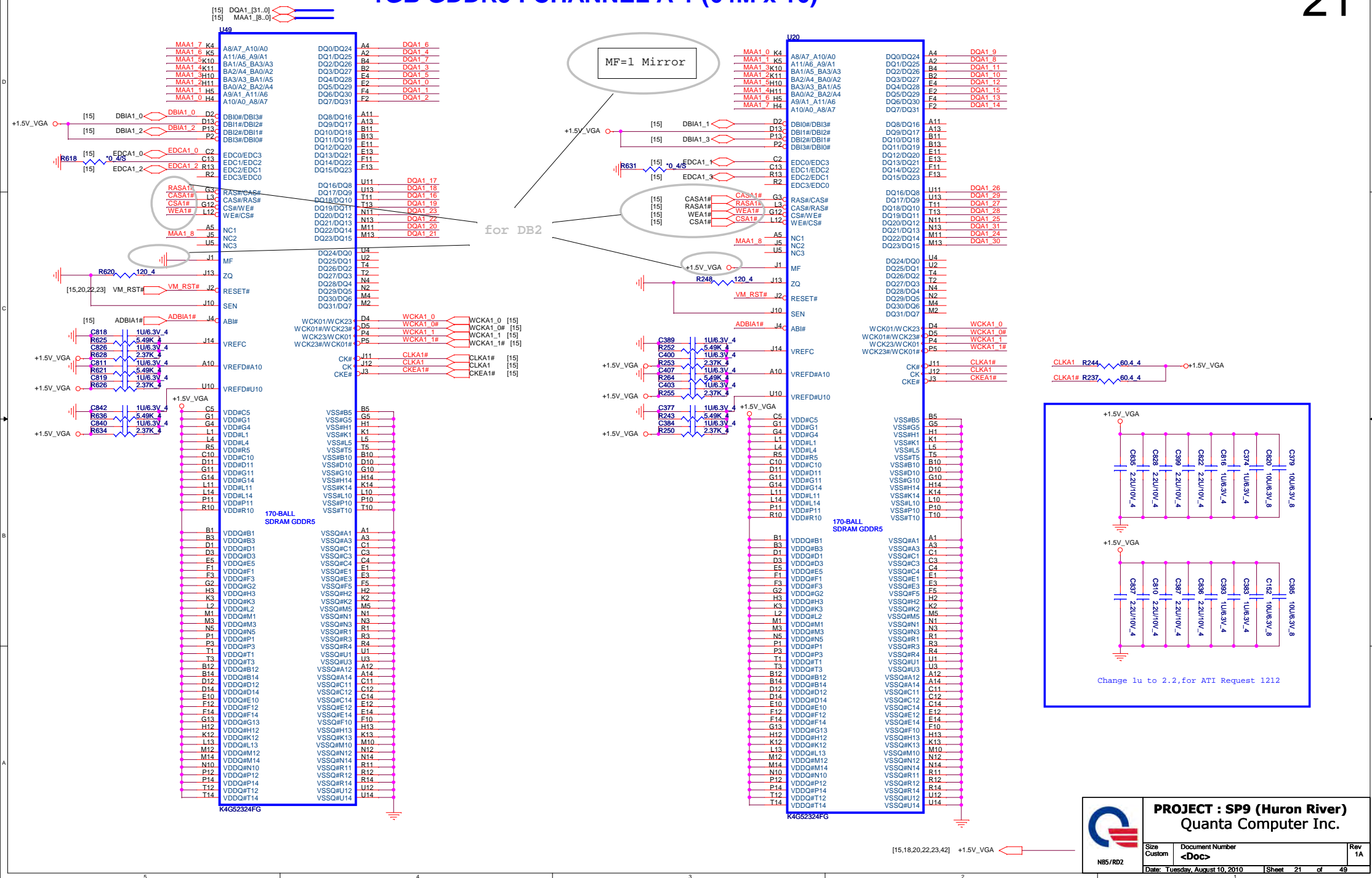
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number VGA Core/+1.8VGFx/1.0VGFx	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 19	of 49

1GB GDDR5 : CHANNEL A-0 (64M x 16)

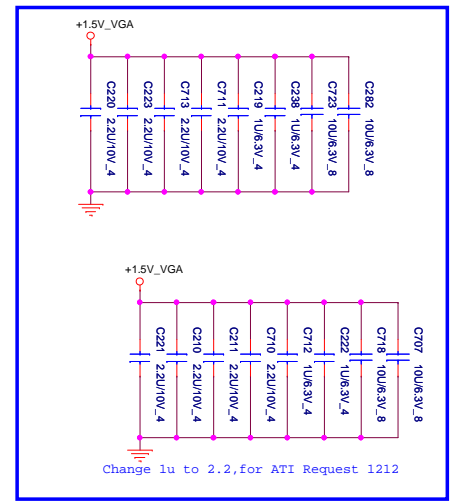
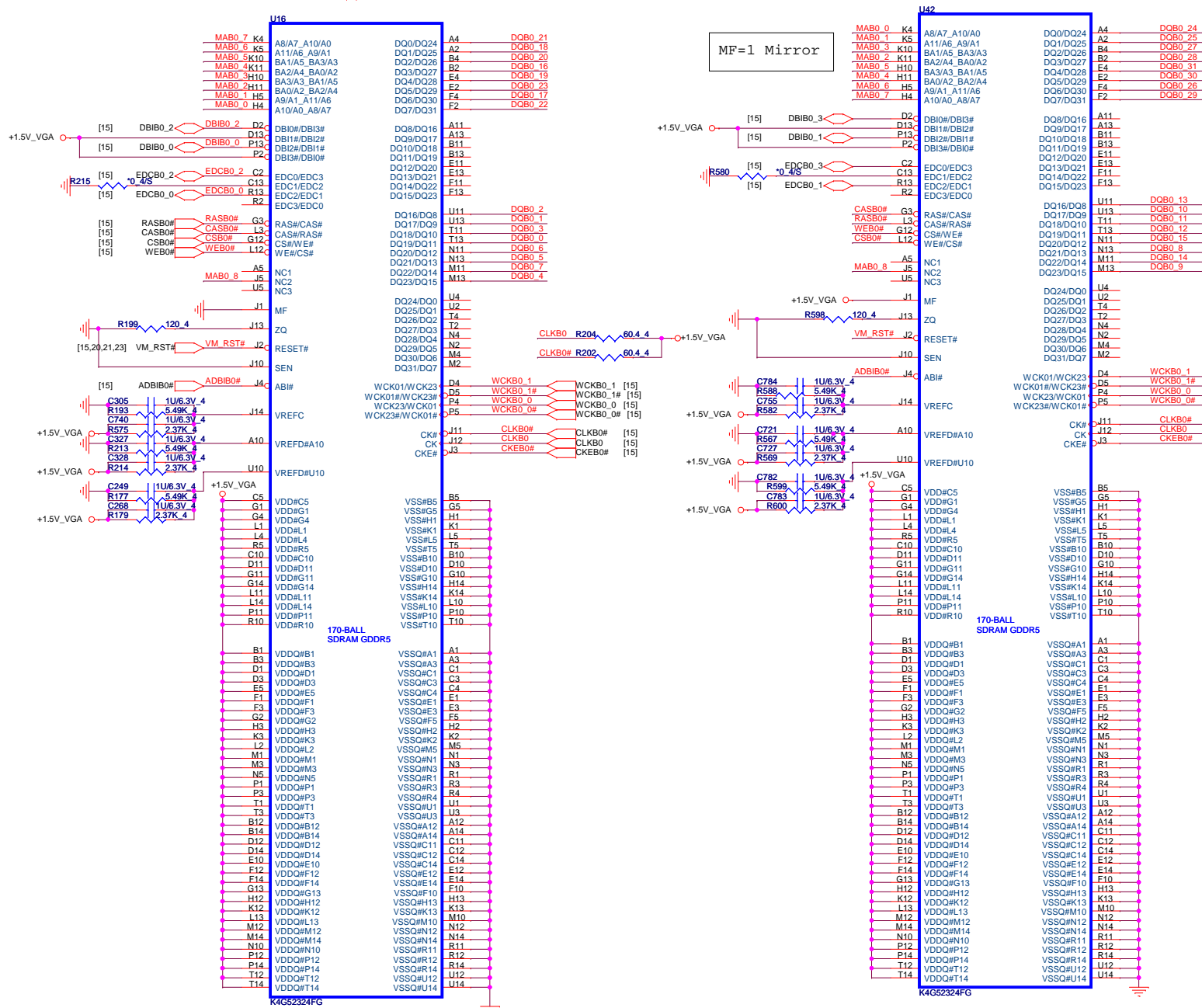


1GB GDDR5 : CHANNEL A-1 (64M x 16)



1GB GDDR5 : CHANNEL B-0 (64M x 16)

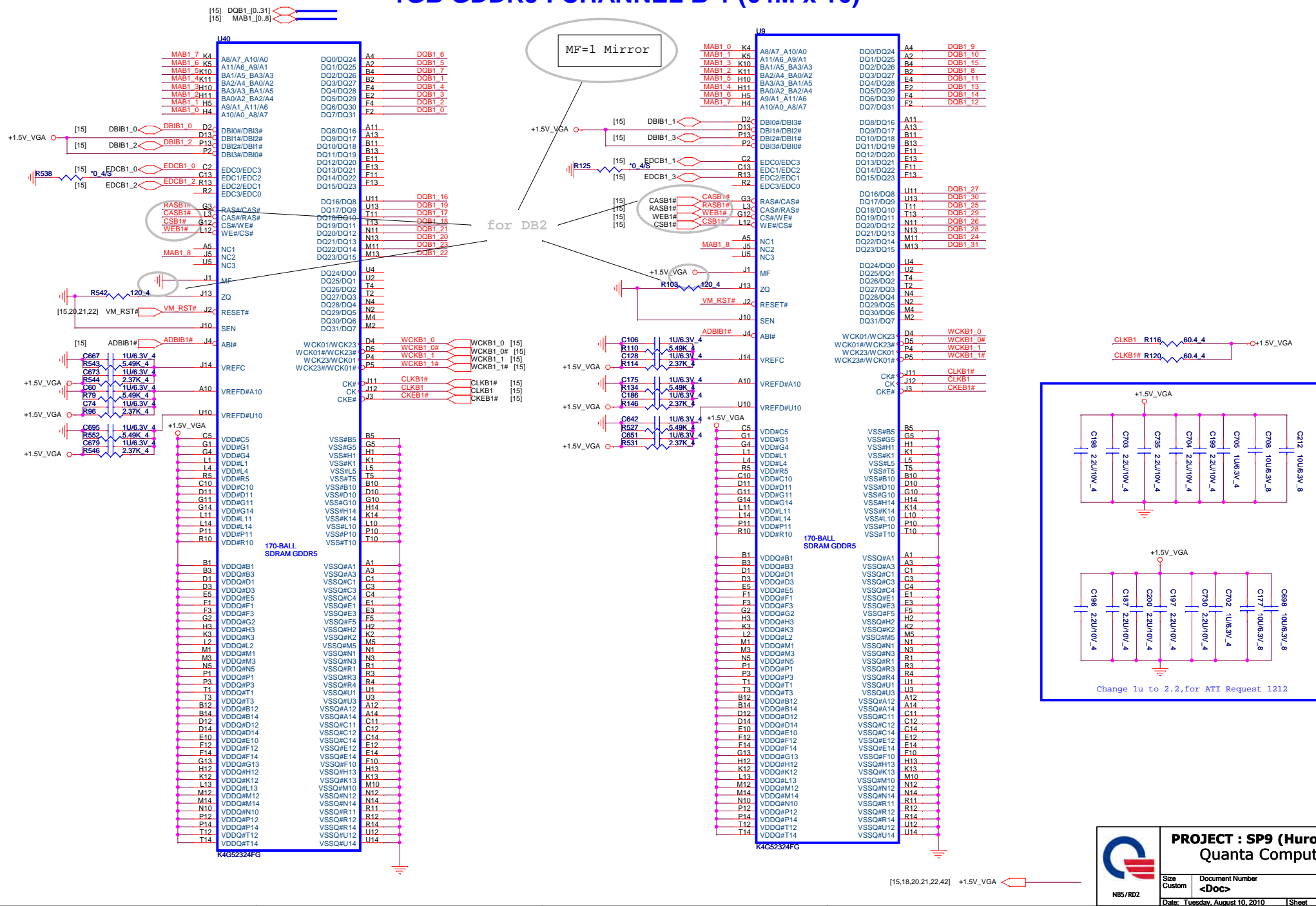
[15] DOB0_0[0..31]
[15] MAB0_0[0..8]



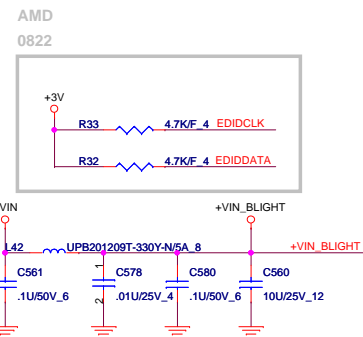
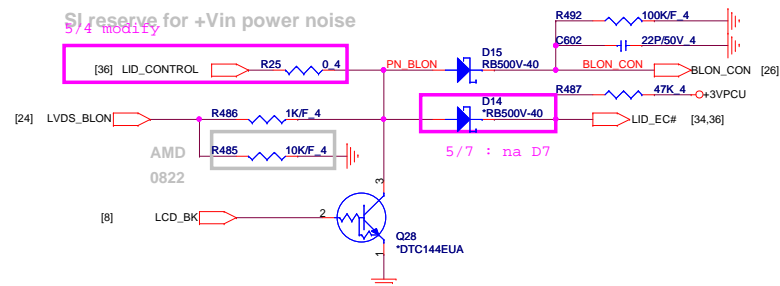
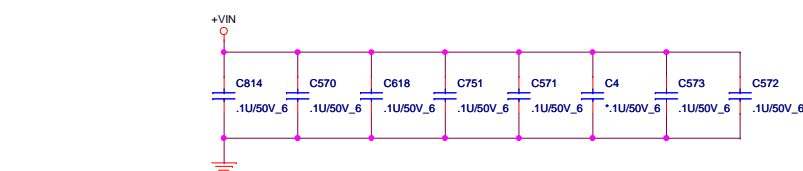
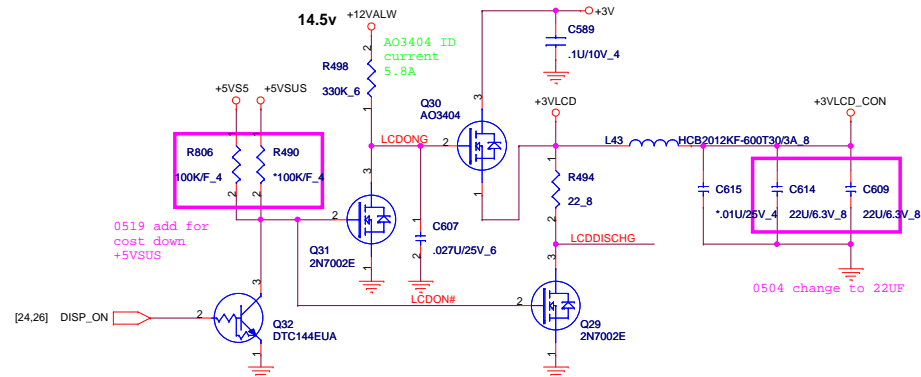
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 22 of 49	

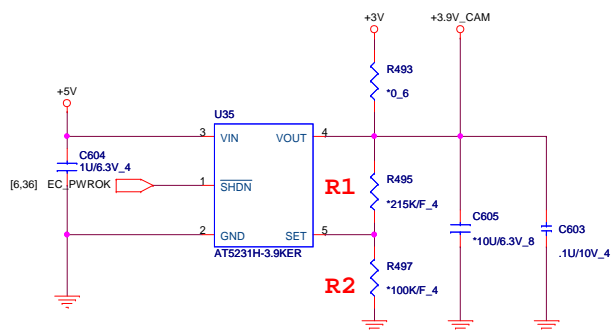
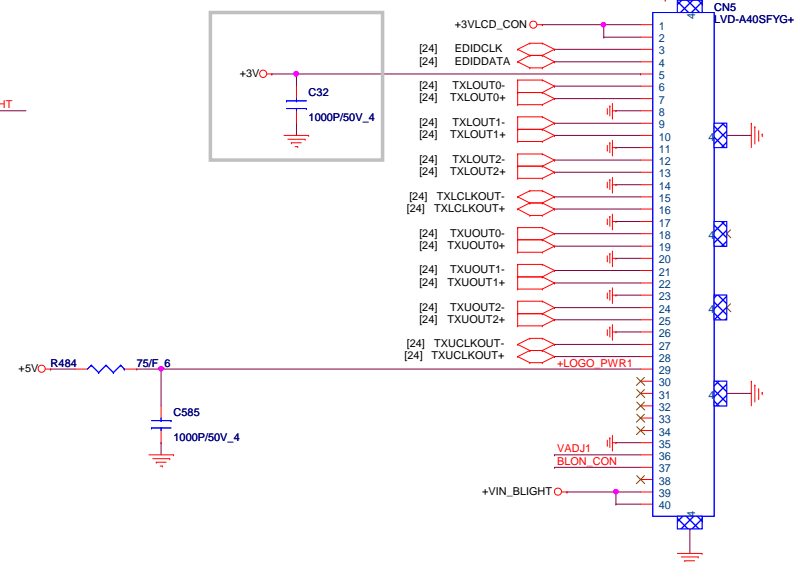
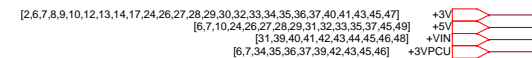
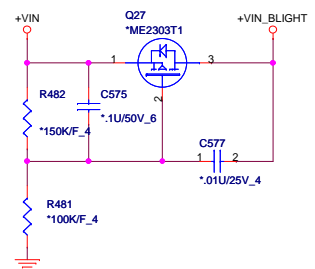
1GB GDDR5 : CHANNEL B-1 (64M x 16)






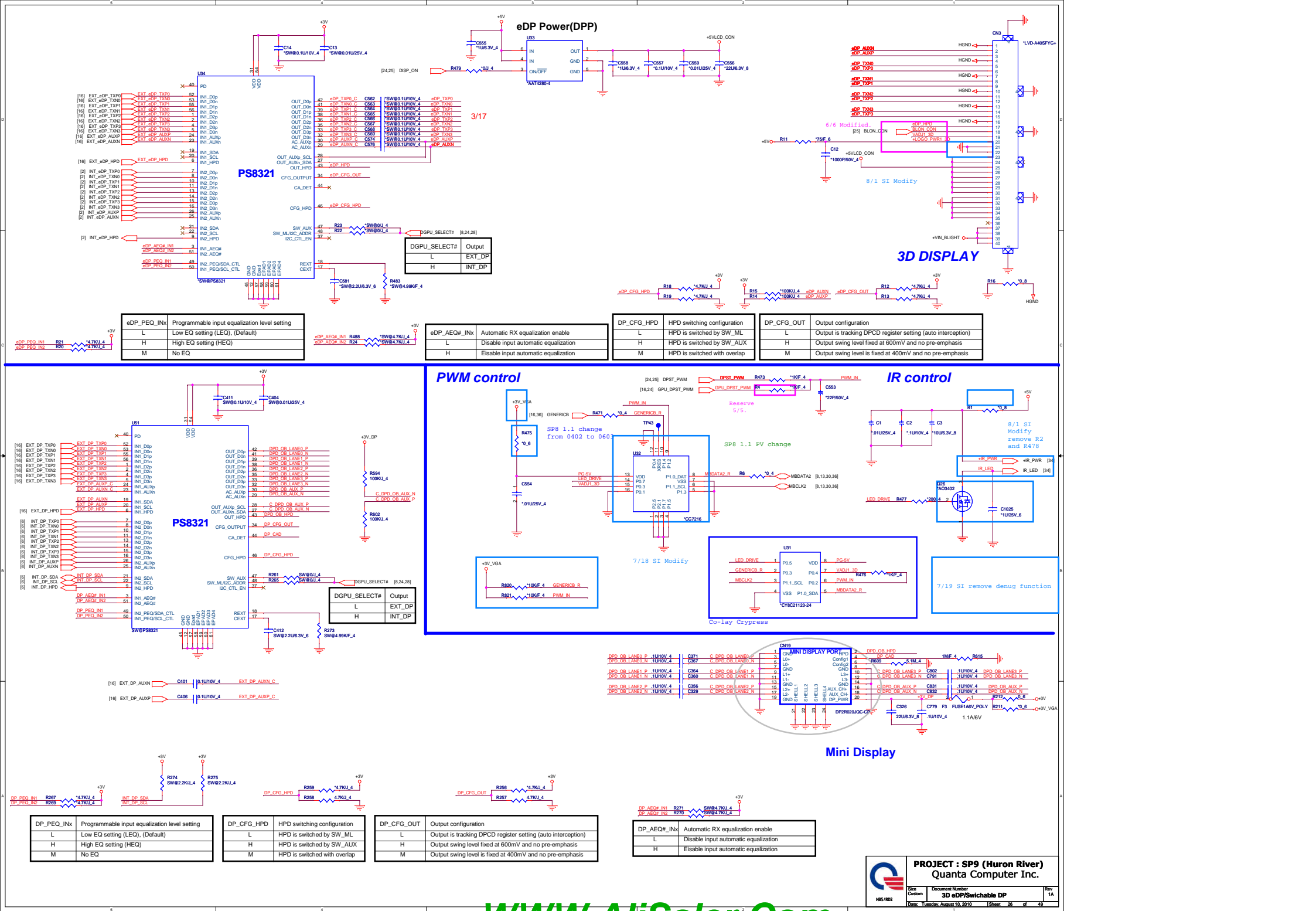


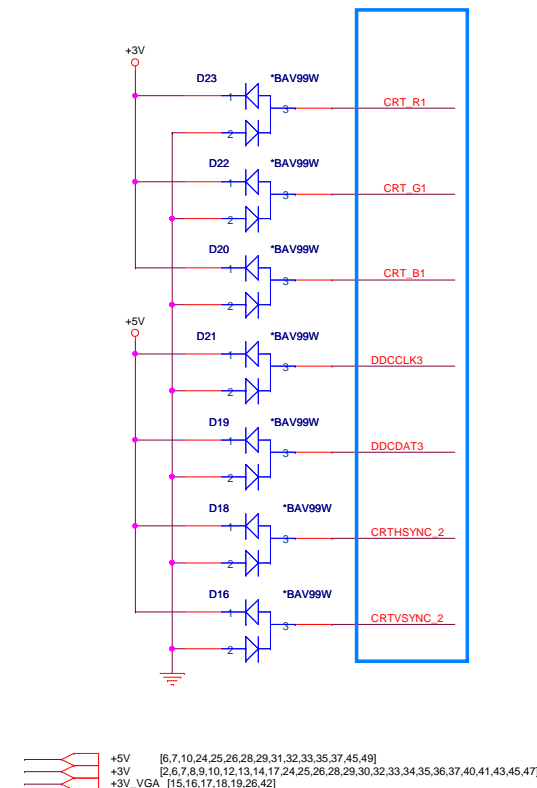
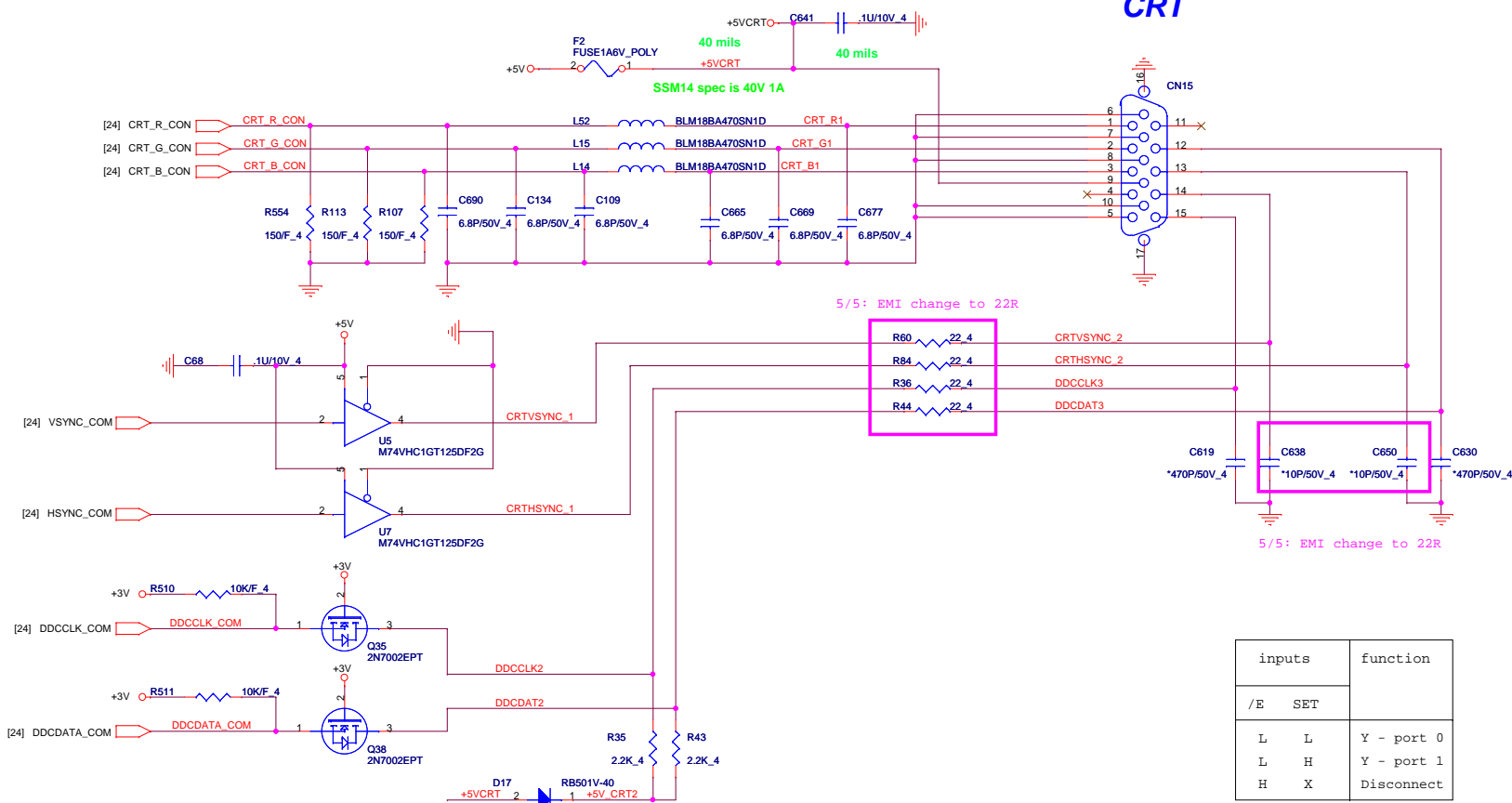
SI reserve for LCD soft start circuit



$$V_{out} = 1.25(1 + R1/R2)$$

	PROJECT : SP9 (Huron River)		
	Quanta Computer Inc.		
Size Custom	Document Number	LCD CONN/LID function	
	Date: Tuesday, August 10, 2010	Sheet 25	of 49



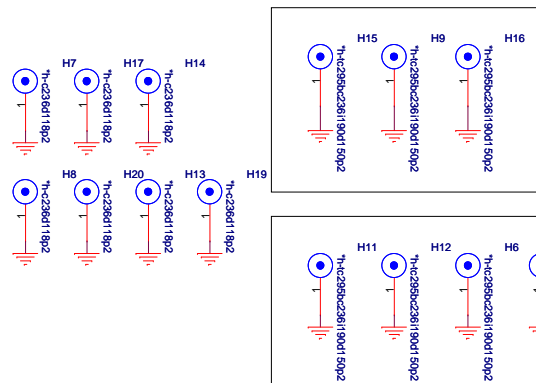


for GPU

SI ME change Footprint

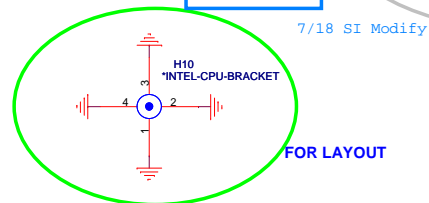
SI for ME change footprint

SI add for PCH hole

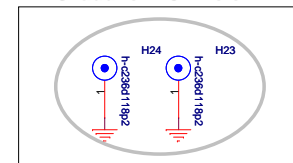



for CPU

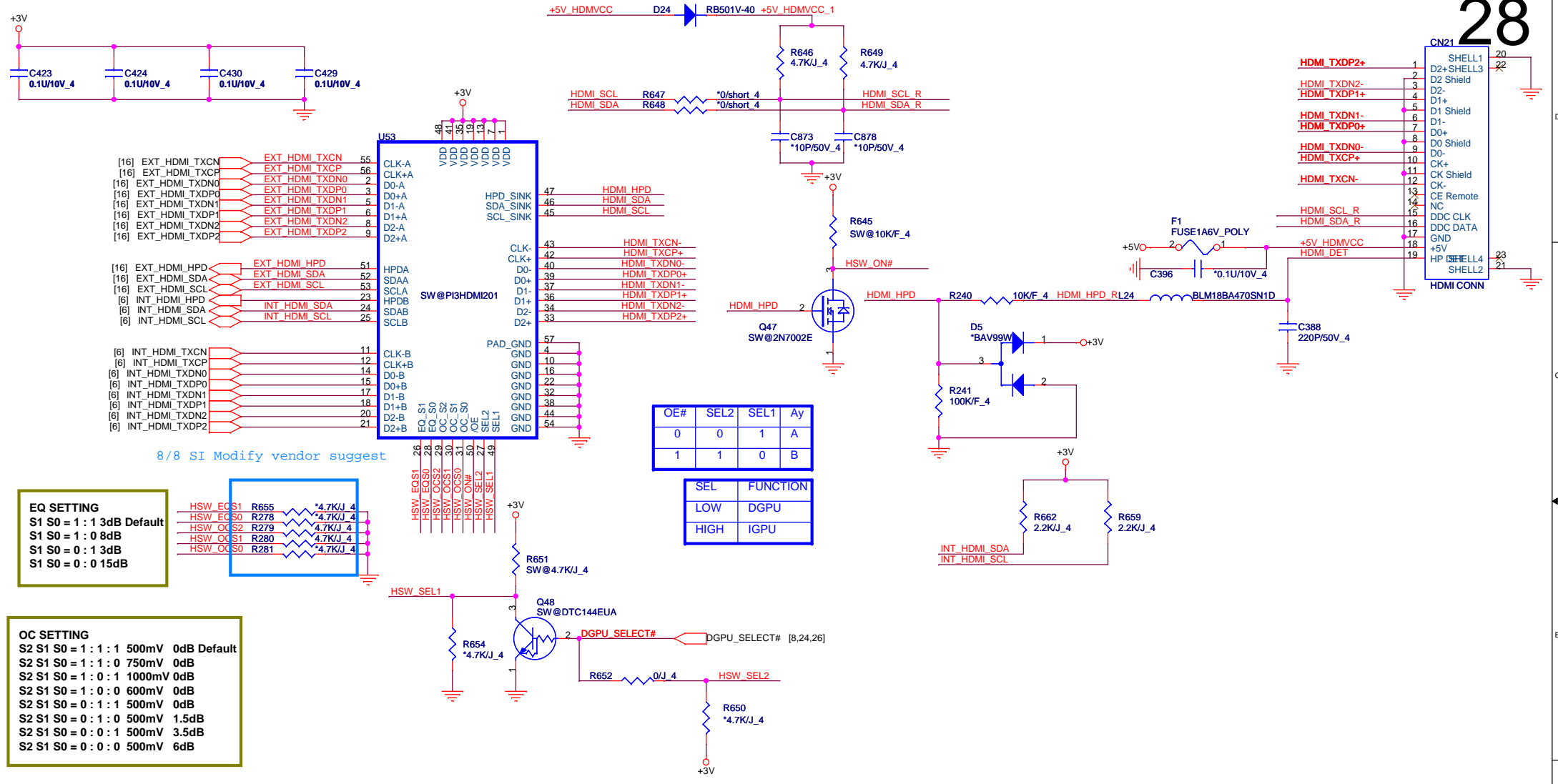
Modify H5\H6,H11\H12\H13\H16\H17,H15 at 0506



HOLDs



 NBS/RD2	PROJECT : SP9 (Huron River)		
	Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
	Date: Tuesday, August 10, 2010	CRT/HDMI Conn	Sheet 27 of 49

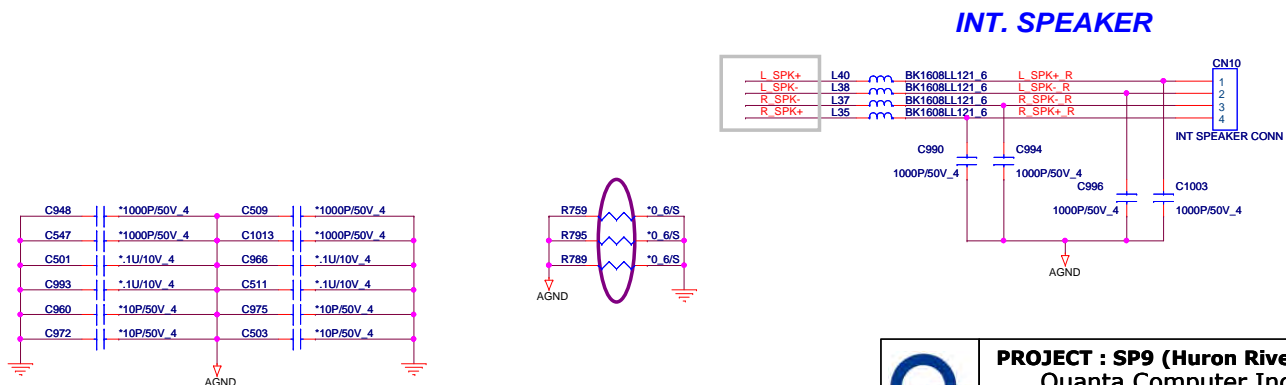
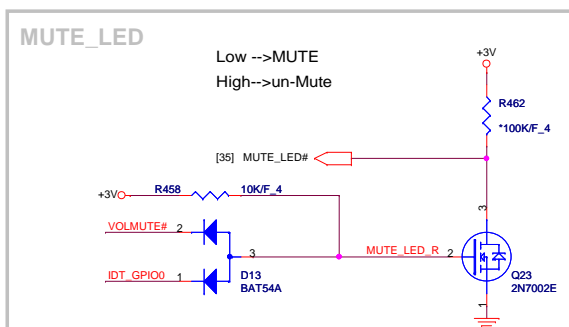
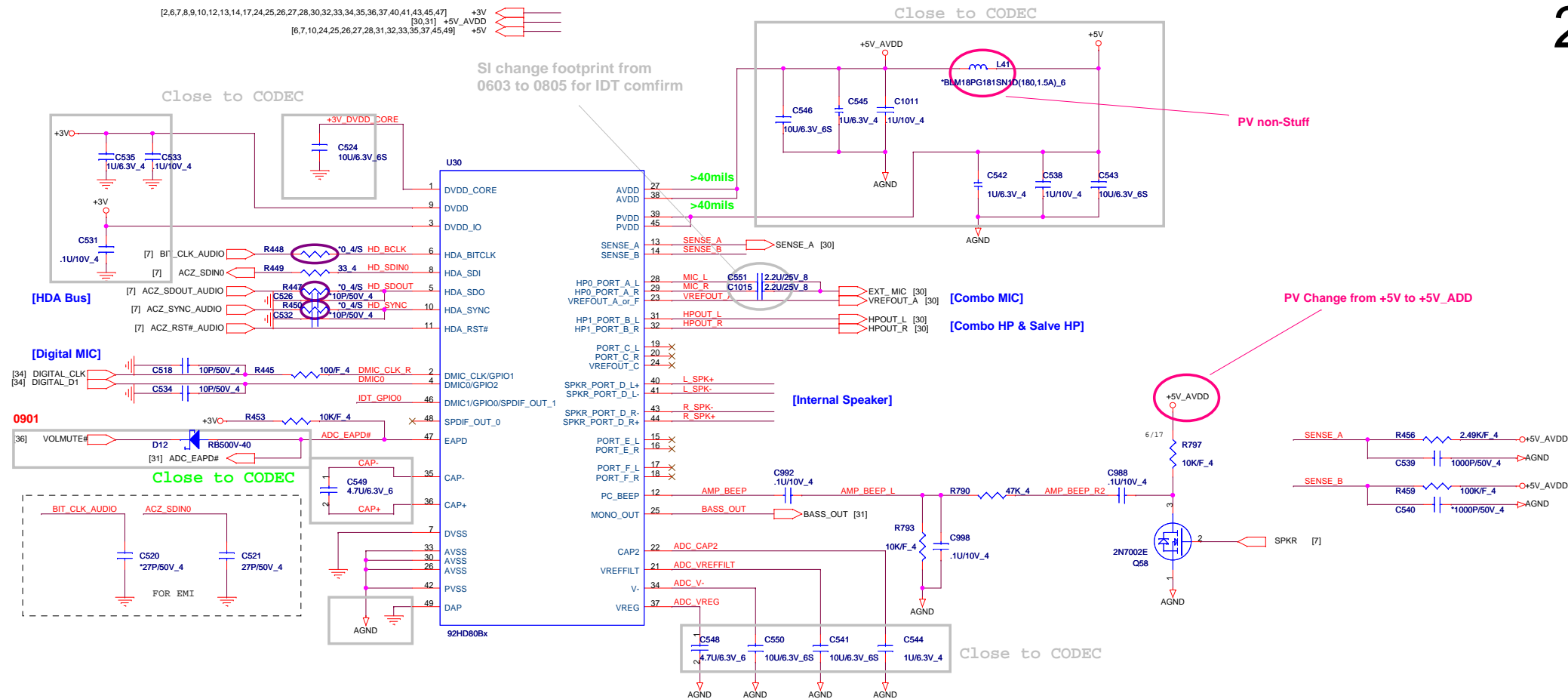



EQ SETTING
 S1 S0 = 1 : 1 3dB Default
 S1 S0 = 1 : 0 8dB
 S1 S0 = 0 : 1 3dB
 S1 S0 = 0 : 0 15dB

OC SETTING
 S2 S1 S0 = 1 : 1 : 1 500mV 0dB Default
 S2 S1 S0 = 1 : 1 : 0 750mV 0dB
 S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
 S2 S1 S0 = 1 : 0 : 0 600mV 0dB
 S2 S1 S0 = 0 : 1 : 1 500mV 0dB
 S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
 S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
 S2 S1 S0 = 0 : 0 : 0 500mV 6dB

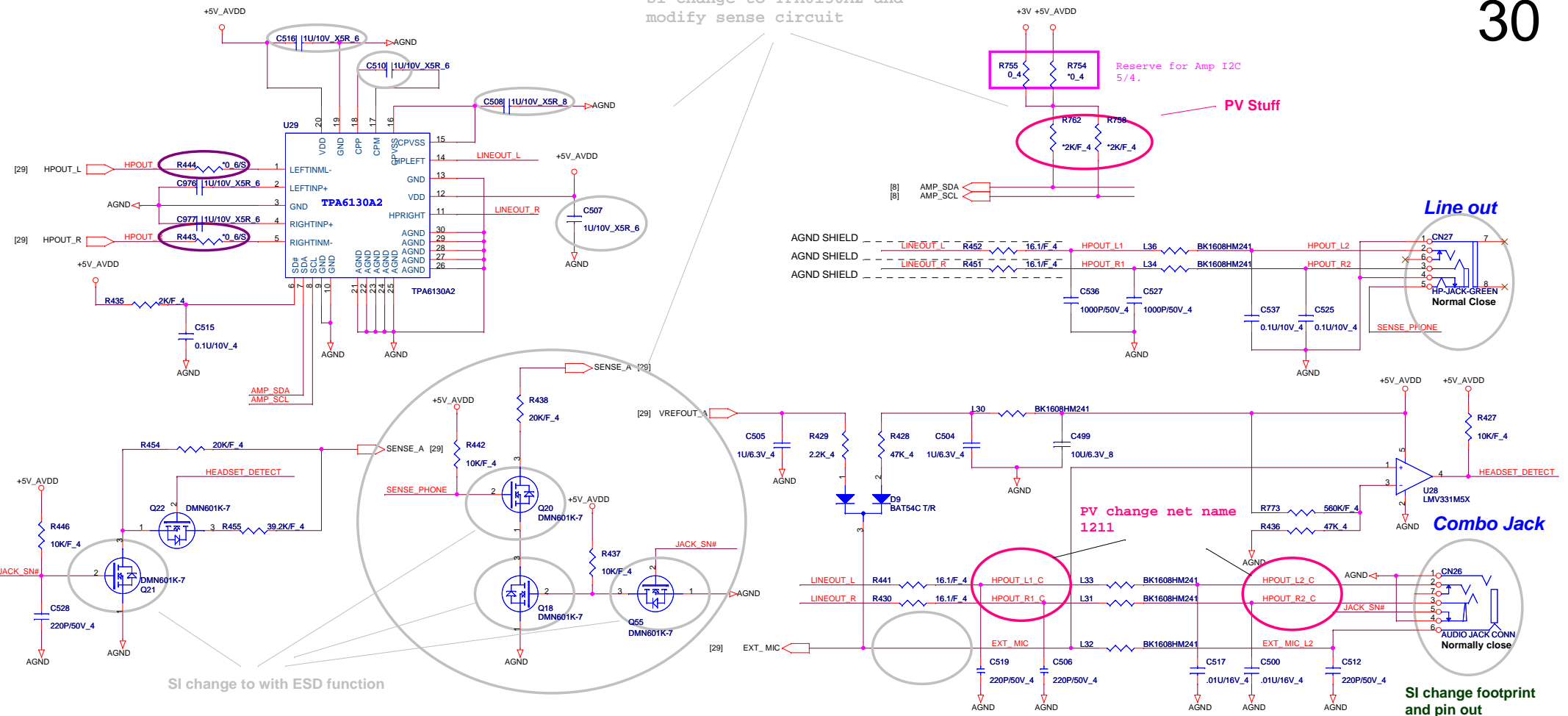
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number SG HDMI Conn	Rev 1A
Date: Tuesday, August 10, 2010		
Sheet 28 of 49		

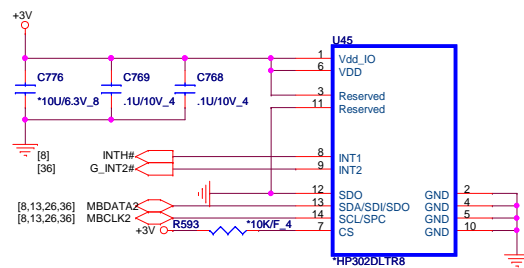


 NBS/RDZ	PROJECT : SP9 (Huron River) Quanta Computer Inc.		
	Size Custom	Document Number Azalia 92HD80	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 29 of 49	

SI change to TPA6130A2 and
modify sense circuit

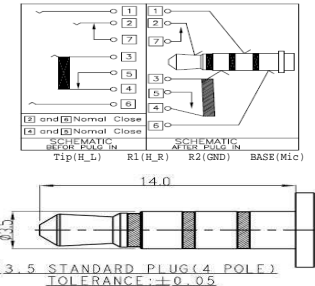
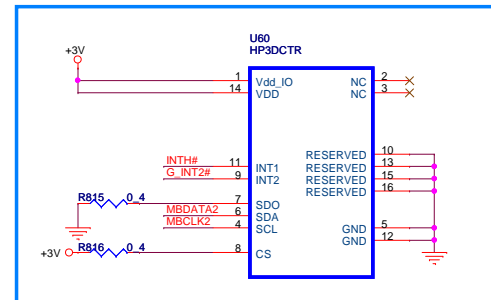


Accelerometer Sensor



Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex

7/18: SI Add



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
N85/RD2	AMP_TPA6047/Accelerometer	
Date: Tuesday, August 10, 2010	Sheet 30 of 49	

SUBWOOFER

31

PV change R575 from 20K to 10K for HP request

SI add LDO for SUBWOOFER power

Change 4EQ to 2EQ

for PV

7/18 SI Modify

close to Connect

Sub-Woofer power


for DB2

MV add R317

GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

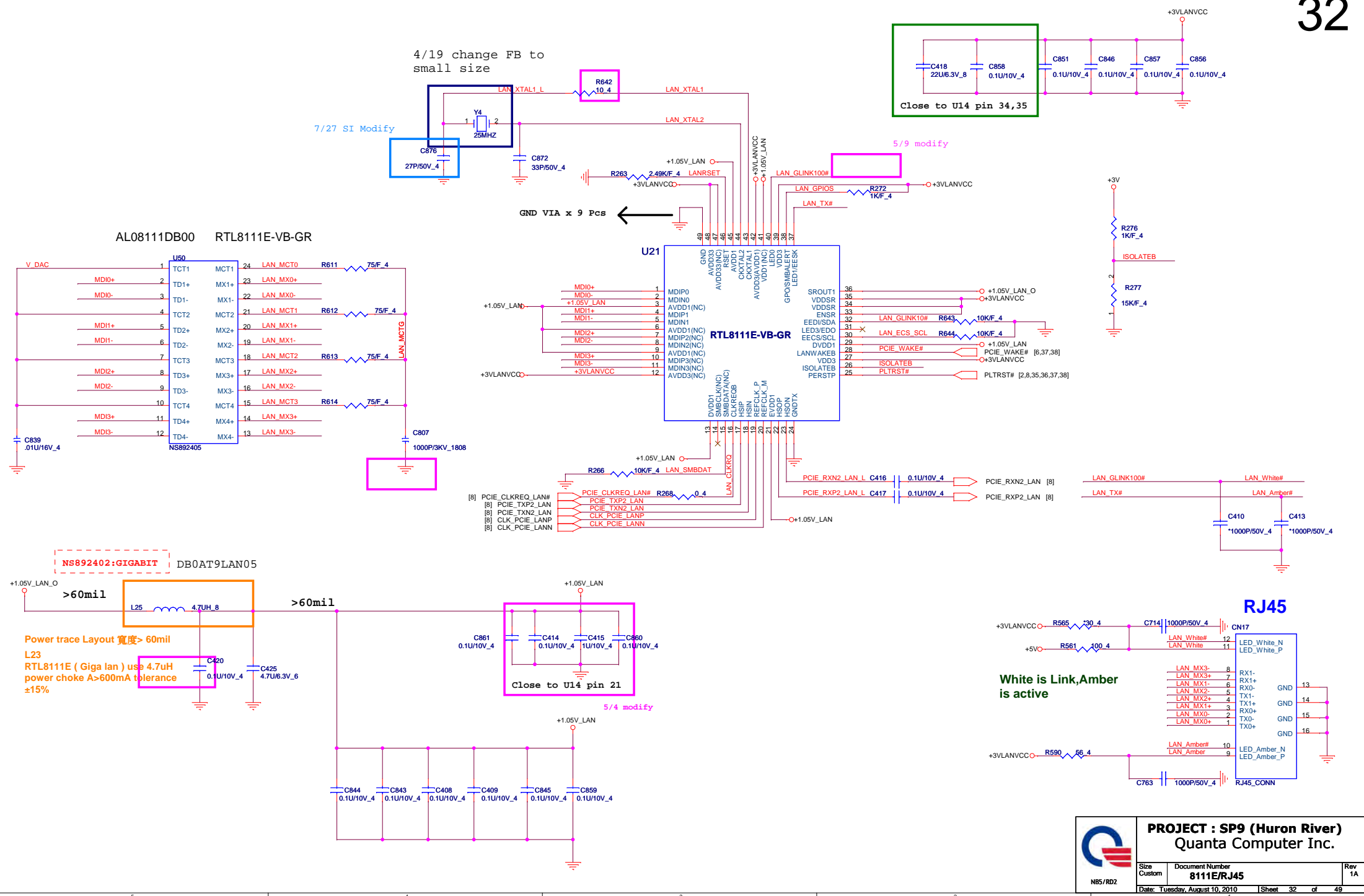
SI change type

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
 +5V_AVDD [29,30]
 +VIN [25,39,40,41,42,43,44,45,46,48]

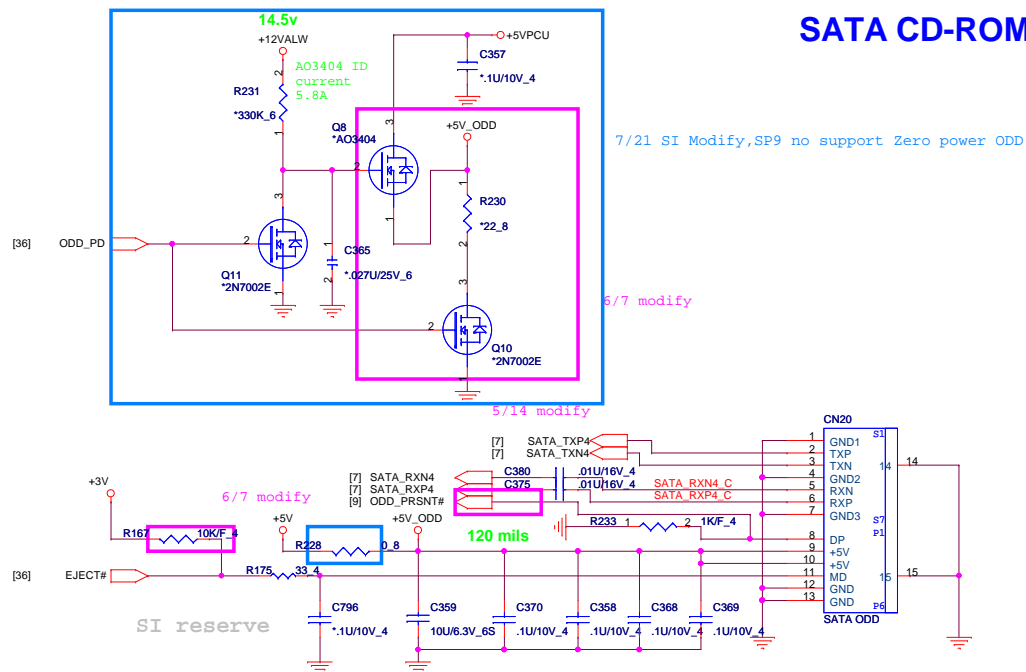


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

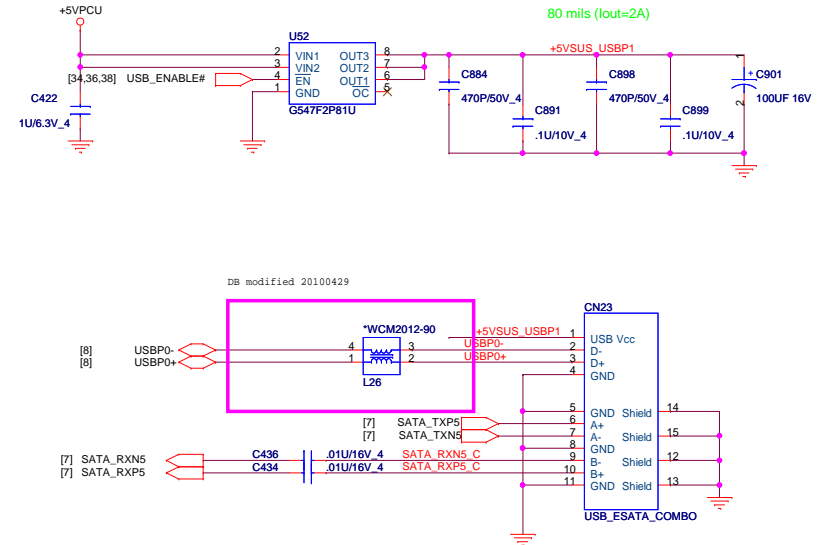
Size Custom	Document Number SUBWOOFER (EQ & AMP.)	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 31	of 49



SATA CD-ROM

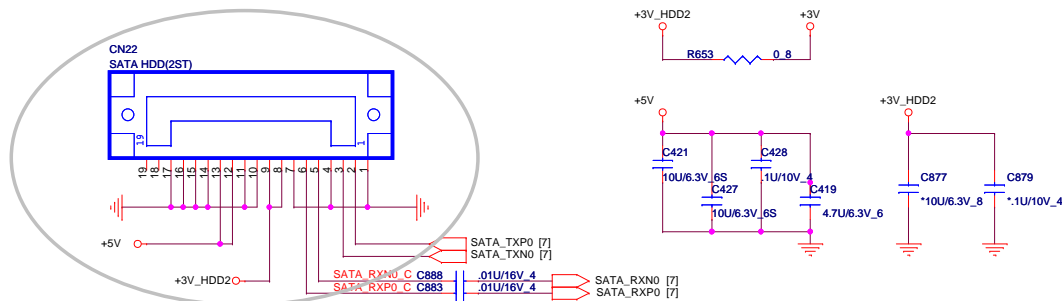


E-SATA



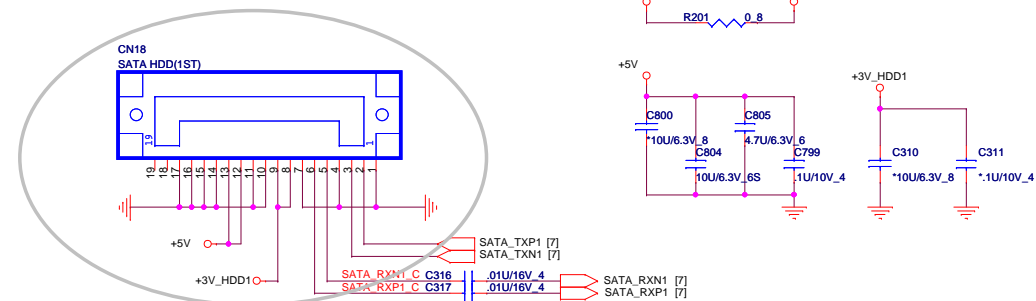
SATA HDD #1

SI change pin define and footprint (the same AX)



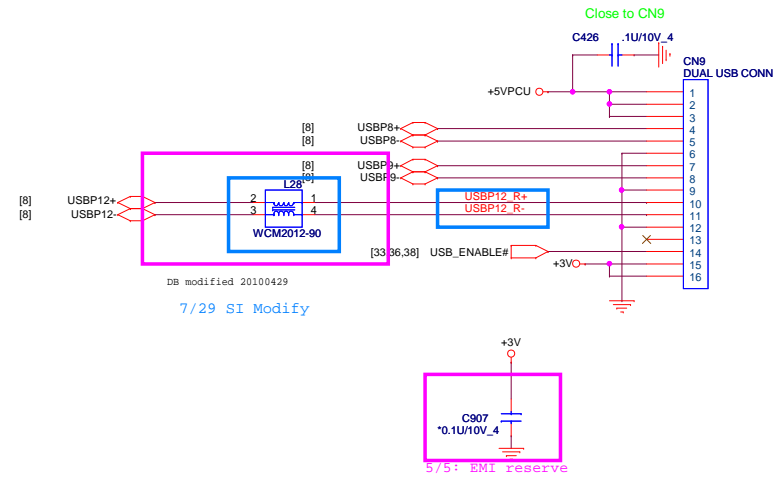
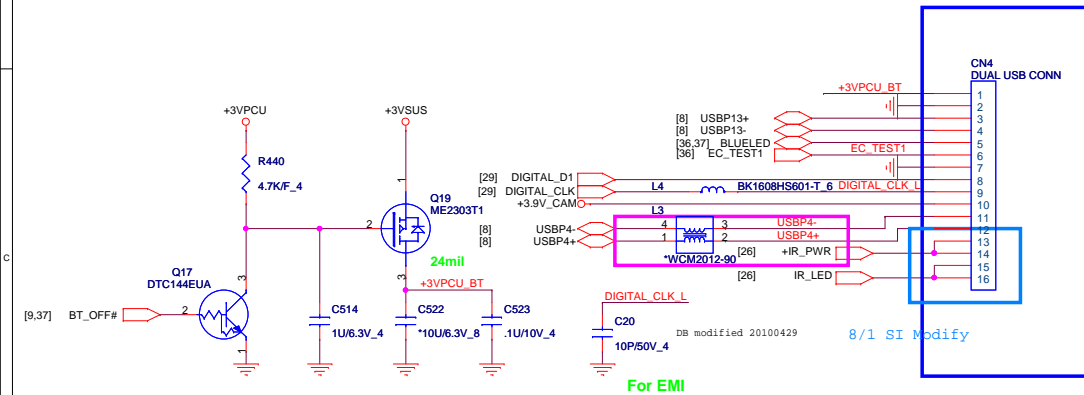
SATA HDD #2

SI change pin define and footprint (the same AX)



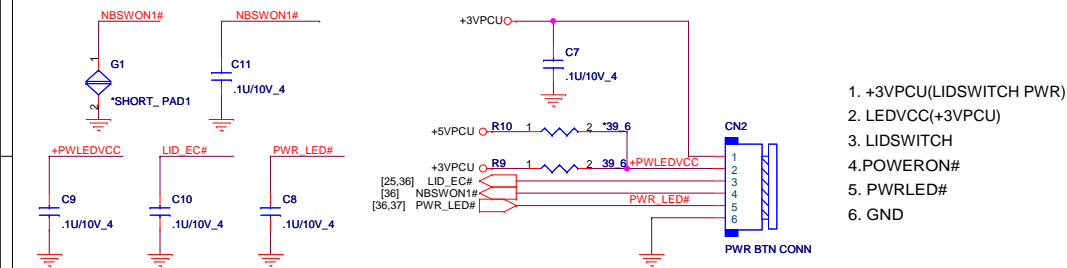
Bluetooth

Ext USB & Card Reader

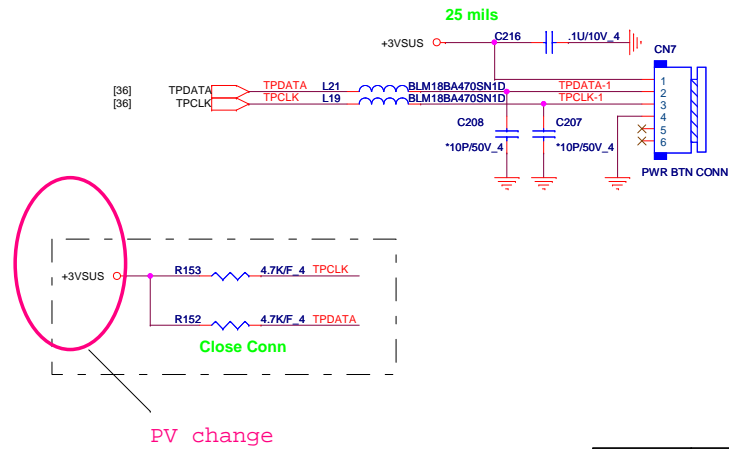


Power Button

Touch Pad Button



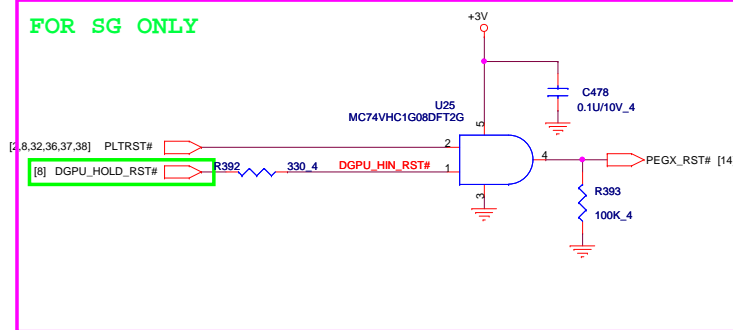
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



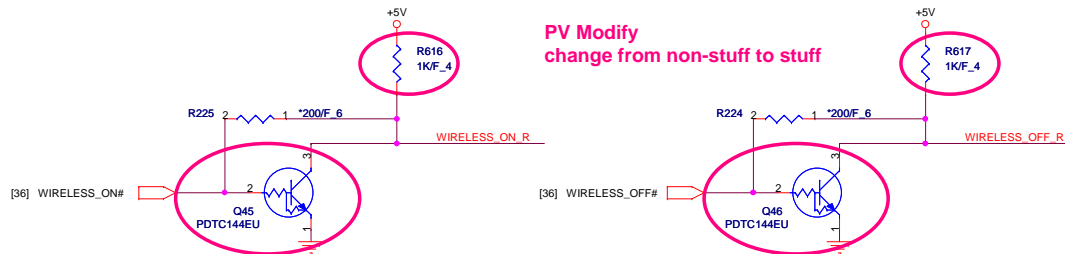
Mini Display

35

FOR SG ONLY

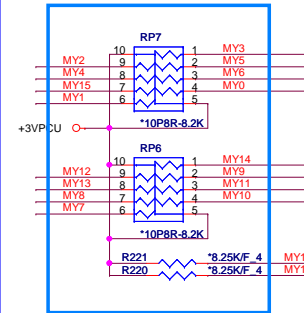


PV Modify
change from non-stuff to stuff

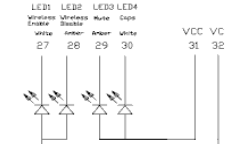
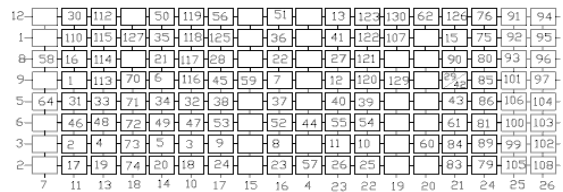
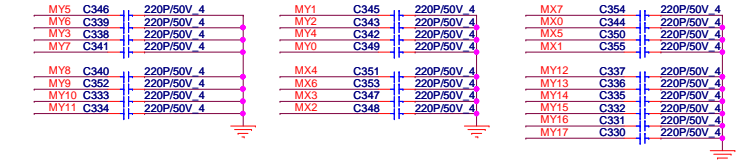
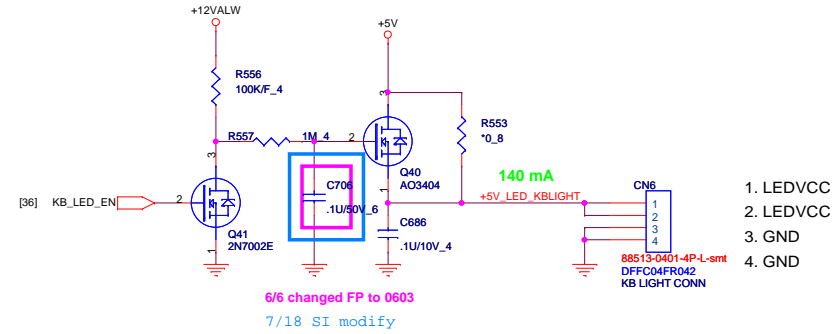
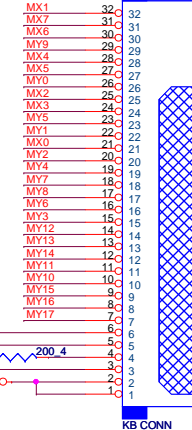


[36] MY[0..17] MY[0..17]
[36] MX[0..7] MX[0..7]

8/5 SI modify

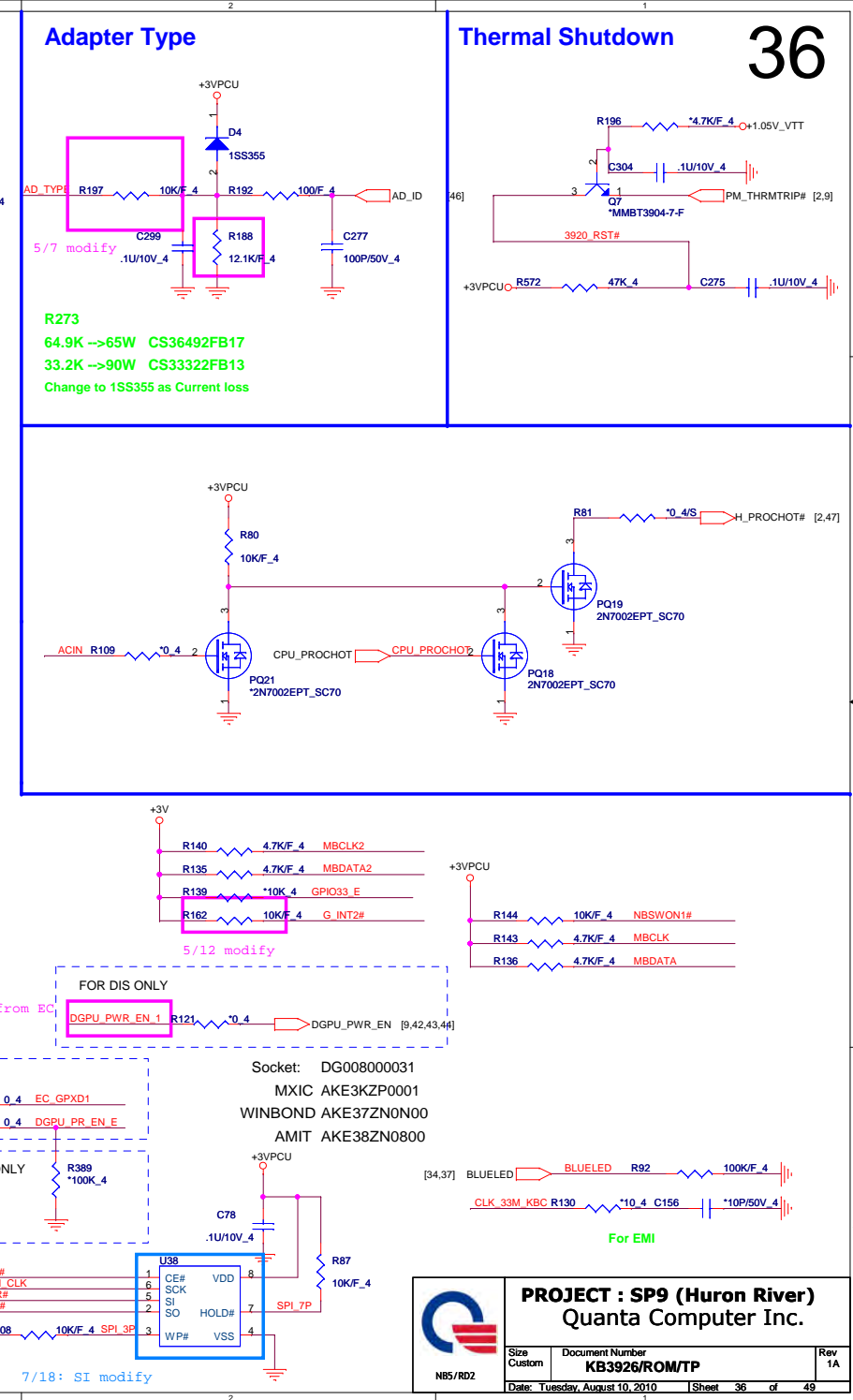
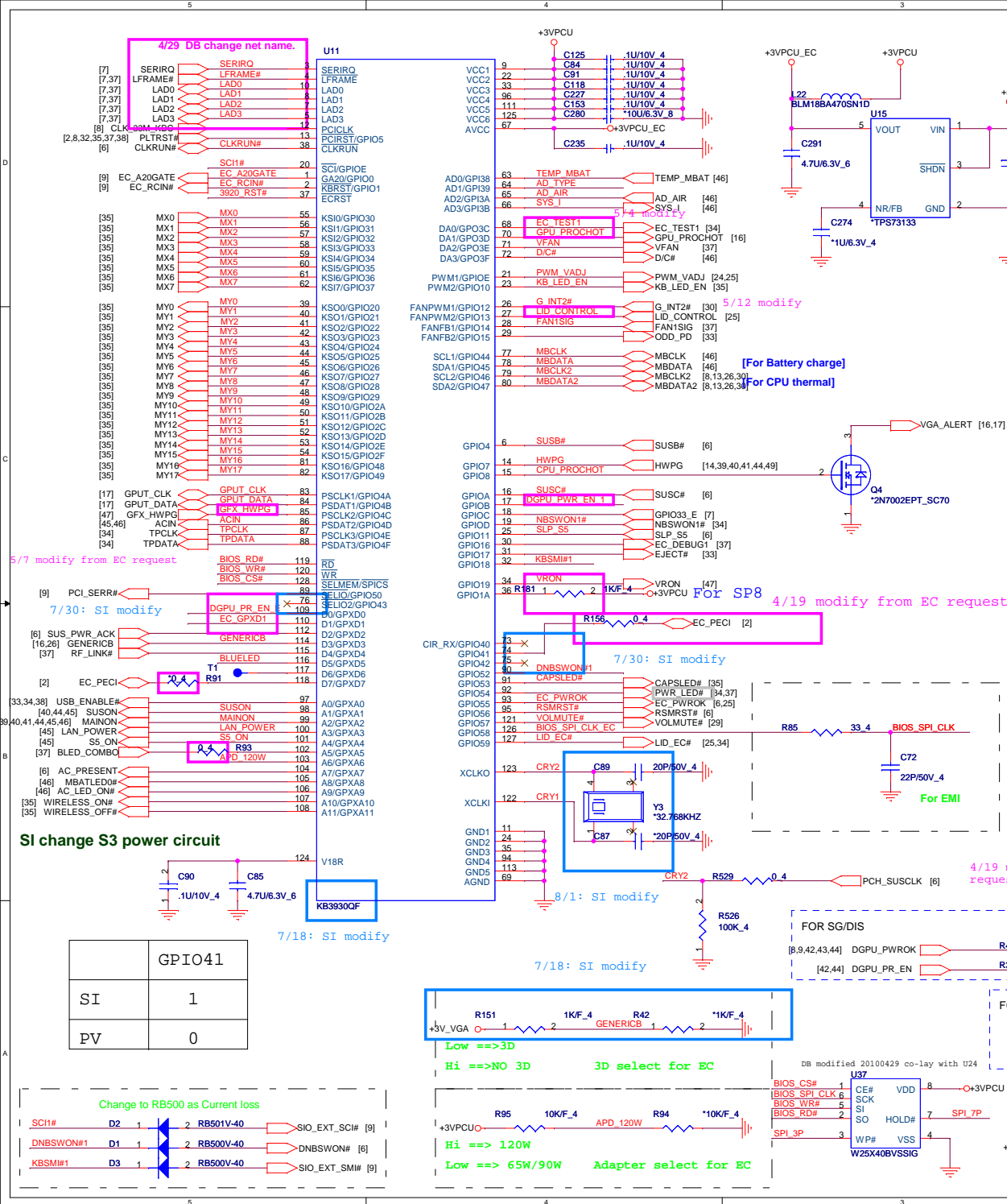


WIRELESS_ON_R
WIRELESS_OFF_R
[29] MUTE_LED#
[36] CAPSLED#
R222 200 4
+3V



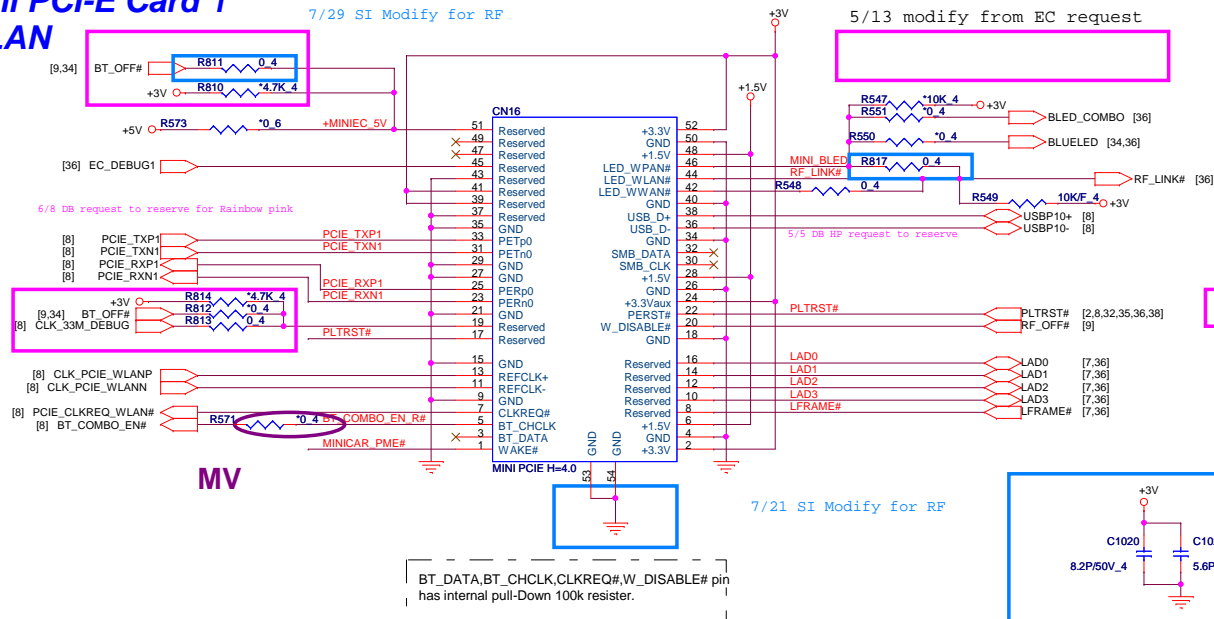
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number KB/LED/POWER CONN	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 35	of 49

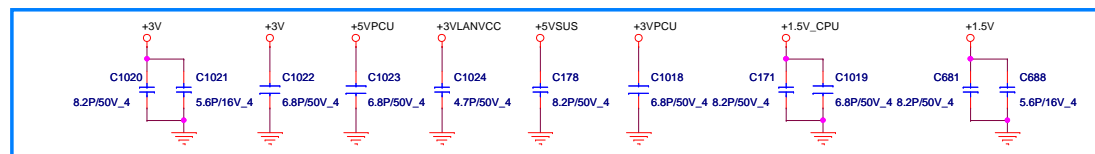
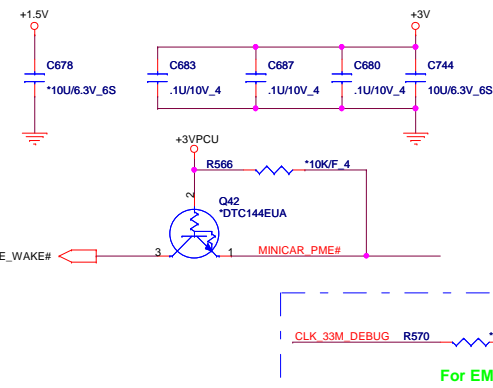


Mini PCI-E Card 1

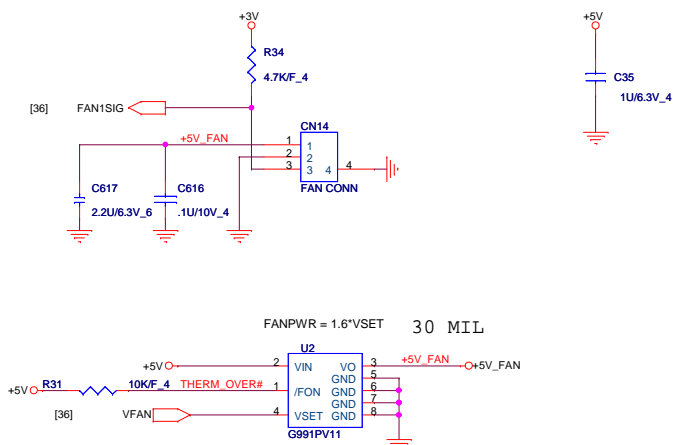
7/29 SI Modify for RF



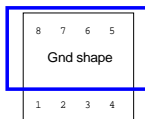
PV non-stuff



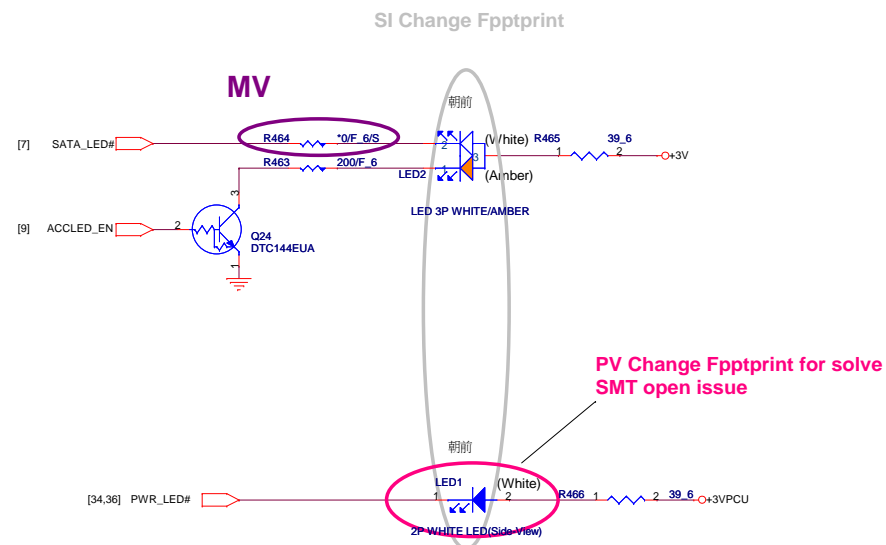
CPU FAN




G995 layout notice



LED

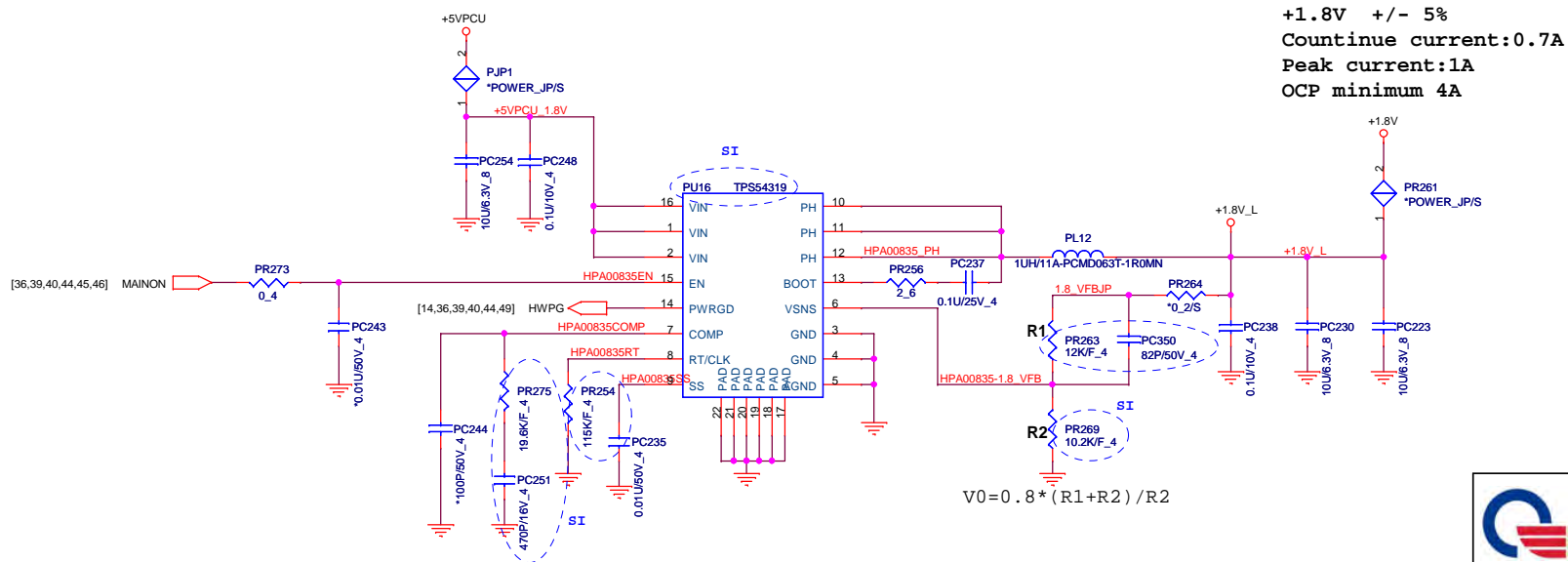
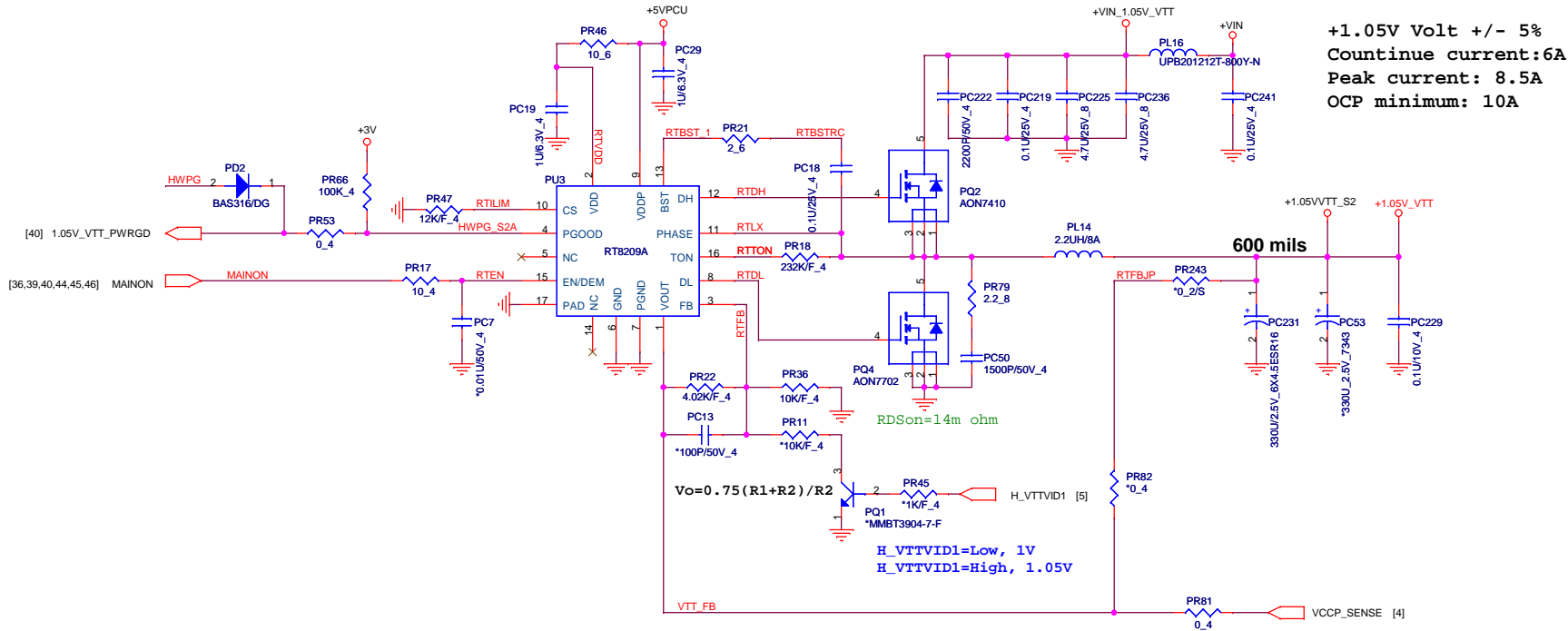


 NBS/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X2	Rev 1A
	Date: Tuesday, August 10, 2010	Sheet 37 of 49	



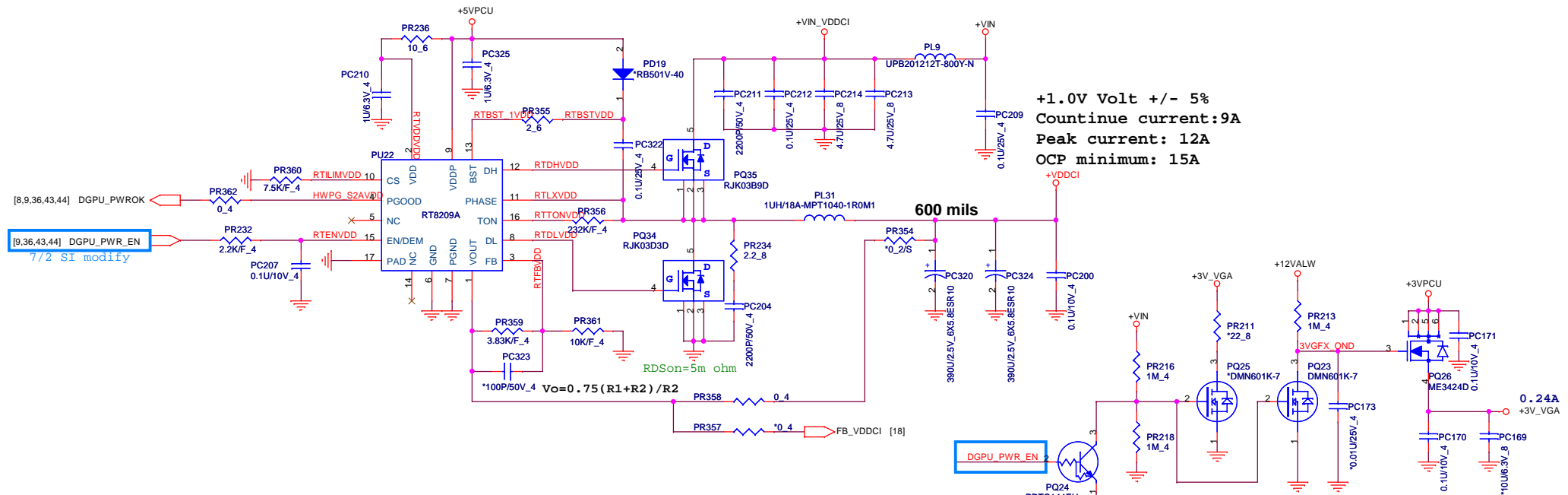




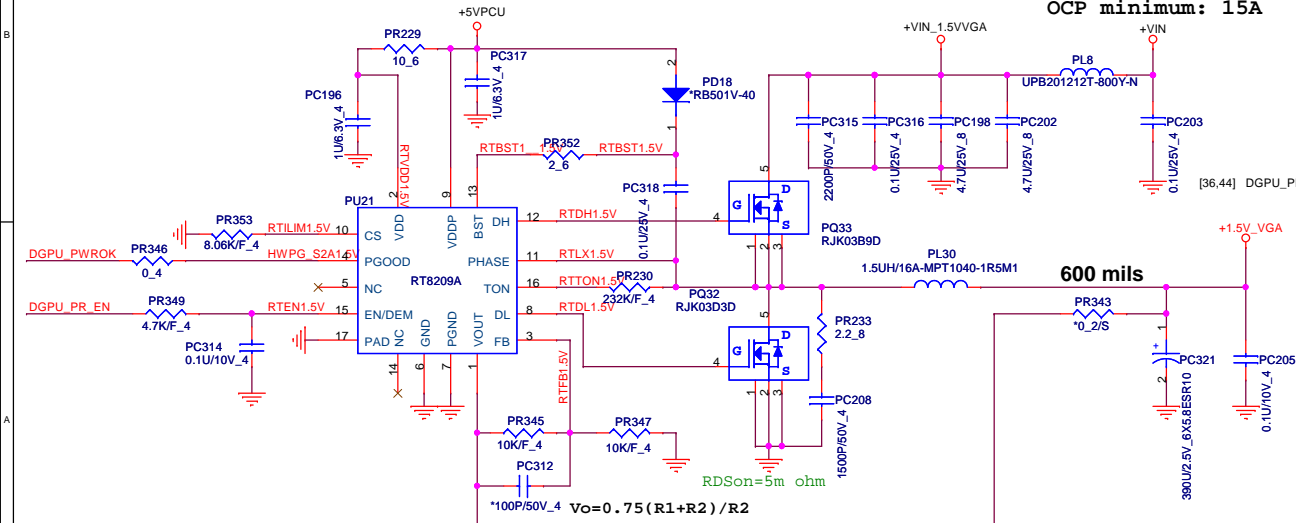
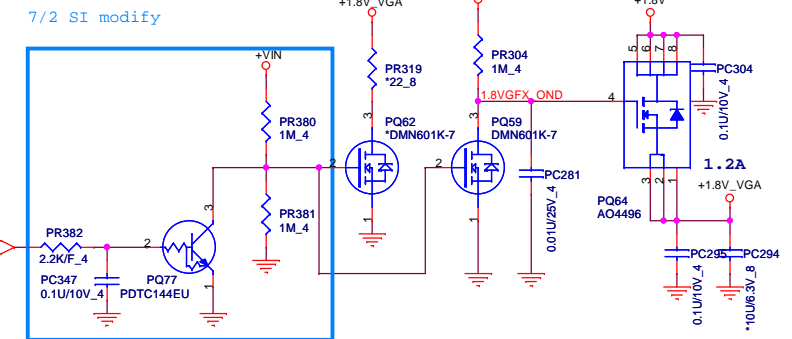


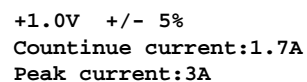
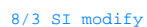
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

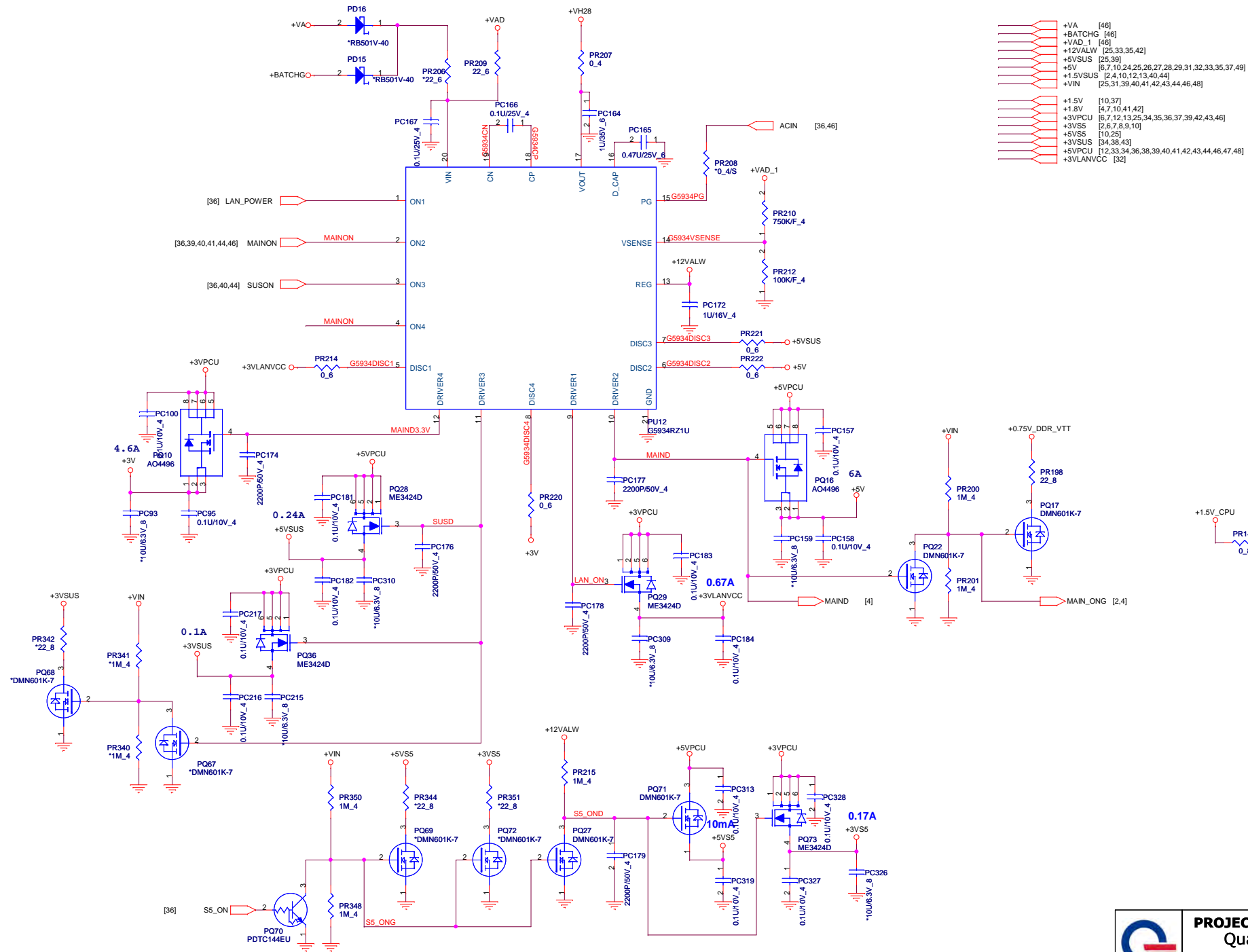
Size Custom	Document Number +1.05V/+1.8V (RT8204C)	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 41 of 46	



+1.5V Volt +/- 5%
Countinue current: 9A
Peak current: 12A
OCP minimum: 15A



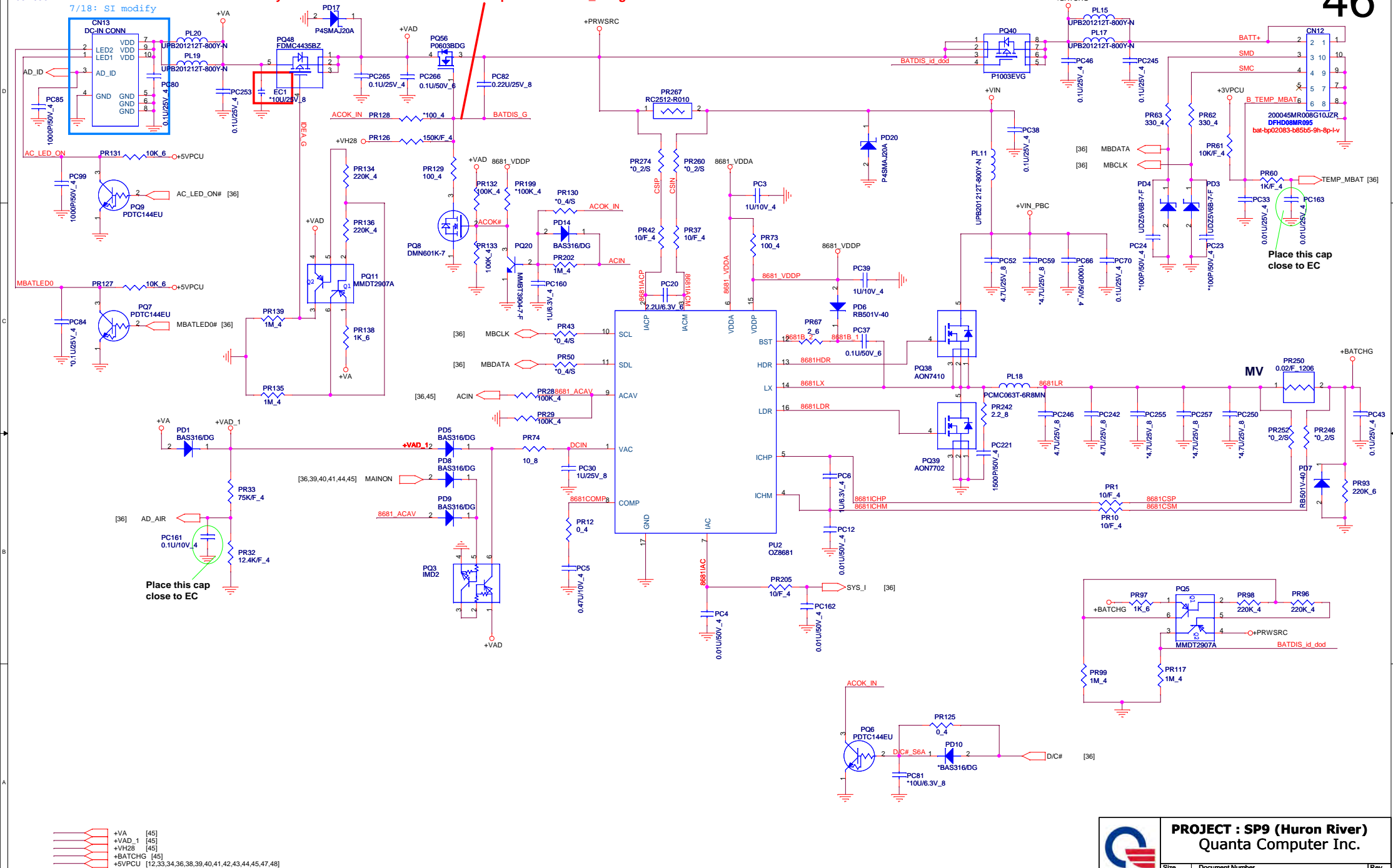




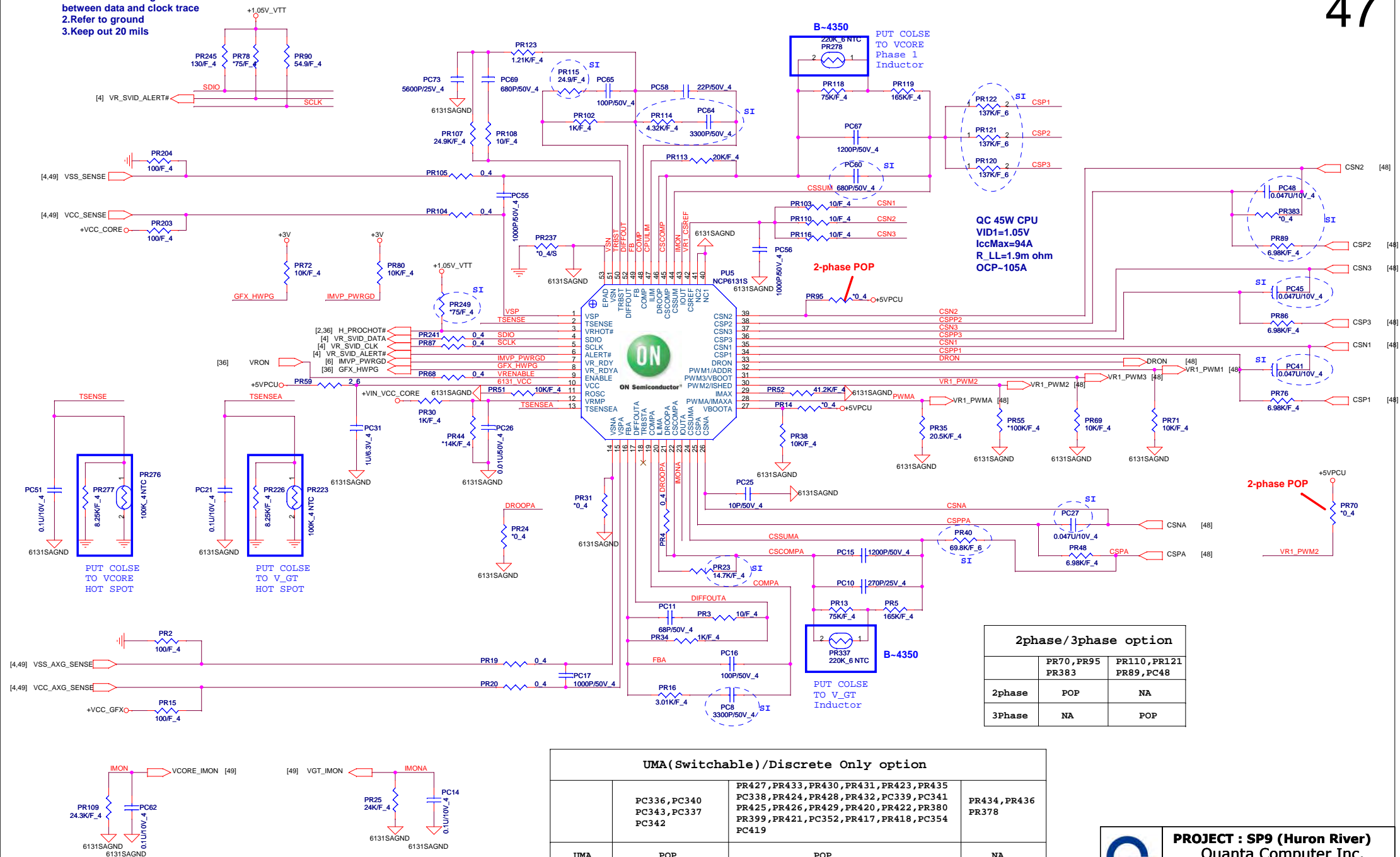
TOP DC_JACK
65W/90W

For EMI test only no stuff

Do Not add test pad on BATDIS_G signal

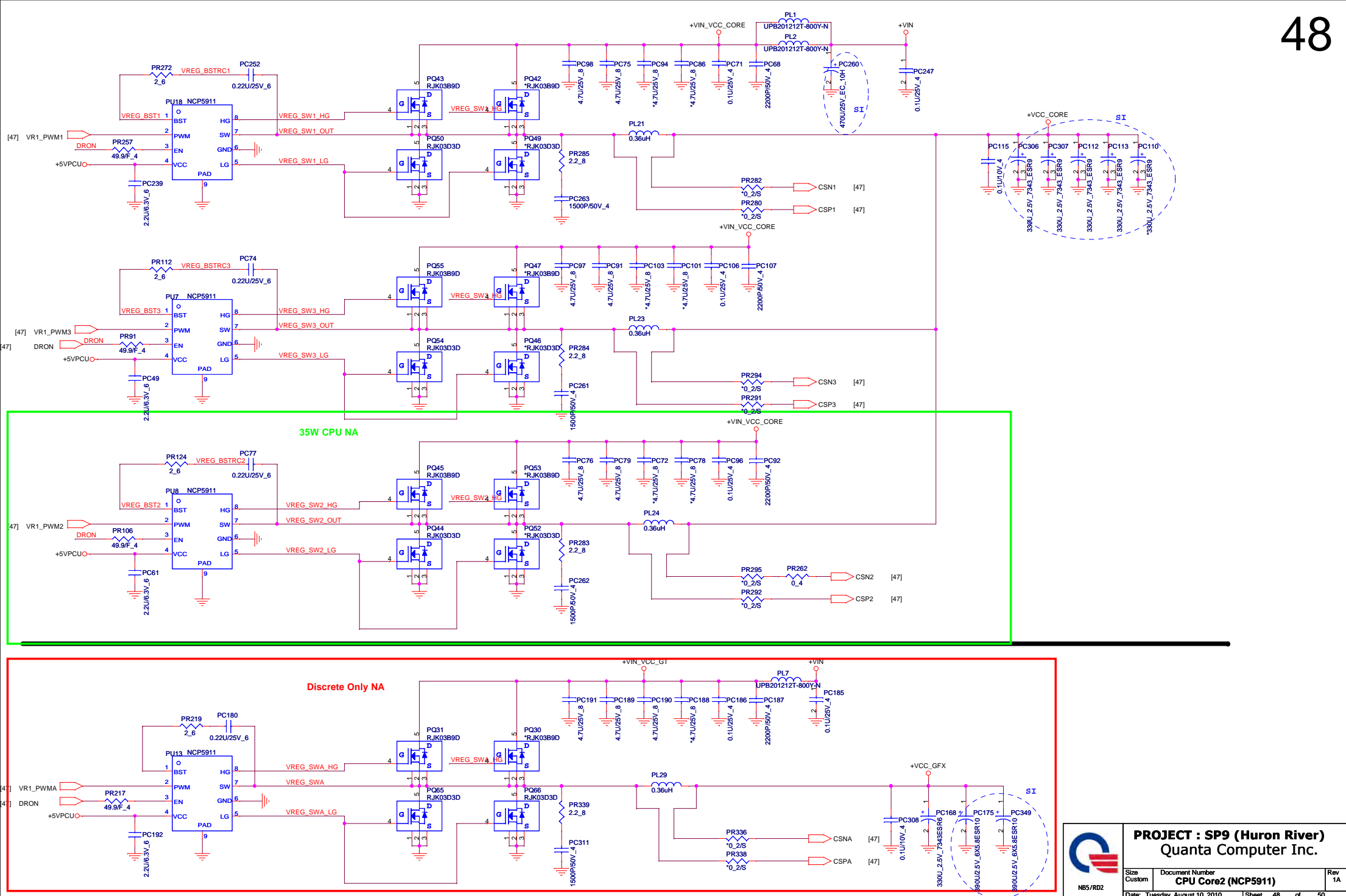


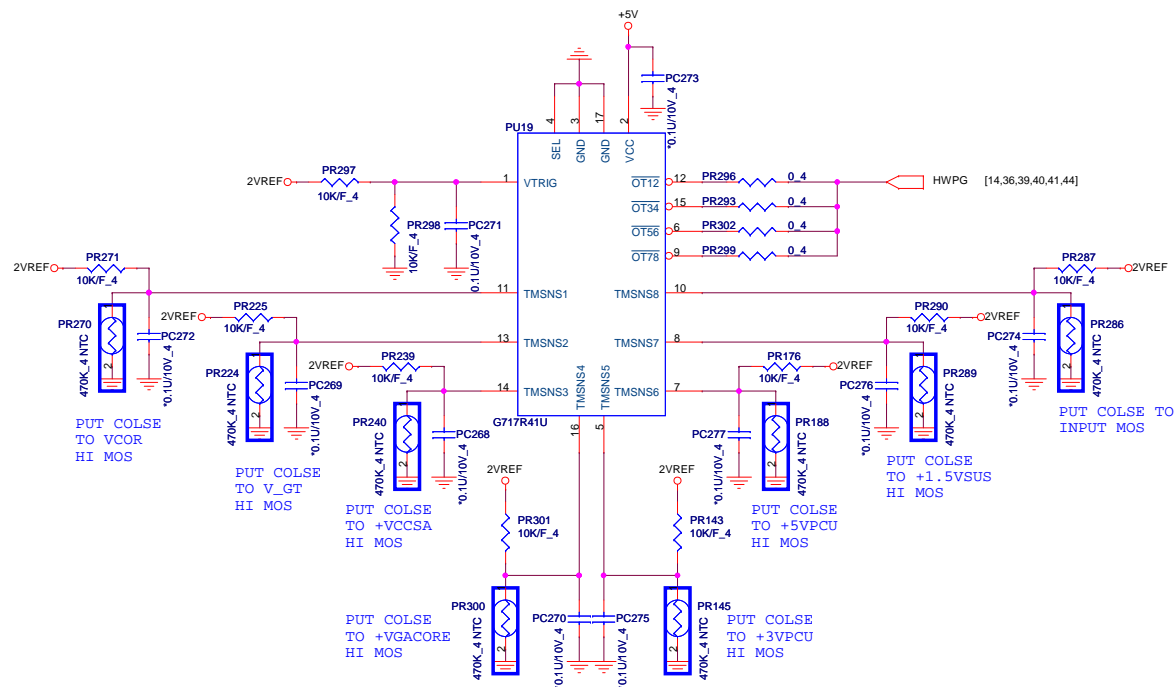
- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom Document Number CPU Core1 (NCP6131S) Rev 1A
Date: Tuesday, August 10, 2010 Sheet 47 of 46





Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031